EPRC – 12
Project Proposal

Cu Pillar Interconnect and Chip-Package-Interaction (CPI) for Advanced Cu Low K chip

15th Aug 2012
Introduction: Motivation / Challenge

- Silicon device with ultra low k material has increased concern on Chip-Package-Interaction (CPI) effect which can potential causing damage to chip during assembly and reliability.

- Increased adoption of Cu pillar interconnect for fine pitch Flip Chip for improved performance with higher I/O density.

- Lack of good understanding on CPI effect of package interconnect design, materials and assembly processes and the need to explore improved solution for next generation low K chip.

(Source: Infineon)

(Source: AMD)

(Source: Fairchild)
Cu Pillar Technology: Industry Trend

(Source: Renesas, Solid State Technology, May 2012)
Challenges for advanced ultra low K chip with Cu pillar

Stress in Low k layer
Interconnection design, material and process induced stress

Assembly process
Effect of packaging assembly process conditions and sequence

Low K layer structure
Effect of BOEL layout and geometry

Cu pillar design
Effect of Cu pillar structure and solder material

Substrate effect
Substrate design and material properties

Underfill materials
Material properties and process condition

(Source: Fairchild, ECTC 2010)
Project Proposal

Objective:
Chip-Package-Interaction (CPI) characterization for advanced ultra low K chip (28nm) with Cu pillar interconnect, including the following:

- CPI study on effect of package structure, material and assembly process with Cu pillar including novel design for reduced CPI
- Piezoresistive sensor characterization of chip stresses under assembly and reliability test conditions, on effect of design, material and assembly conditions.
- Mechanical integrity characterization of 28nm low k chip under Cu pillar bump area and correlation with modeling analysis
- EM modeling and characterization for fine pitch Cu pillar interconnect
- Material characterization including fine pitch substrate with low CTE material and pre-applied underfill materials
- Assembly, reliability testing and failure analysis
Test vehicles

**TV1 - FCBGA package**
- Larger chip**, full array bump
- BU substrate with SOP
- Fine pitch bump**
- Low CTE substrate/BU layer
- No flow underfill /pre-applied underfill

** Subject to the 28nm Cu low K chip layout

**TV2 – FCCSP package**
- Smaller chip**, periphery array bump
- 2-layer organic substrate / Si chip substrate
- Fine pitch Cu pillar bump (20um/10um)
- Fine pitch RDL (5um)
- Pad finish (NiAu)
- NUF, NCP, NCF**

**Remark: To be finalized with member’s input and subject to availability**
Stress Measurement using Piezoresistive Stress Sensors

Stress sensor below Cu pillar can be obtained from changes in sensor’s resistance when subjected

•Scope

• Sensor wafer fabrication and testing

• In-situ 4 stress components ($\sigma_{xx}, \sigma_{yy}, \sigma_{zz}, \tau_{xy}$) monitoring during assembly process & reliability test conditions to study effect of package and Cu pillar design, substrate and underfill material type, curing and reliability testing.

(Source: IME Cu wire bond consortium)
Mechanical characterization of Low K chip

**Challenges**

From Low-K to ultra low-k to extreme low-k
  • Cohesion/adhesion strength decreases
  • Modulus decreases
  • Adverse impact on reliability

Understanding of Low K layer integrity is important for the assessment of the interconnect performance

**Possible testing methodologies**

- Bump shear test
- Three-point bend
- Four-point bend

**Approach**

To identify a *feasible and practical test* methodology

To capture the *mechanical integrity* of low-k stacks.

Choice of test depends on the availability of the sample*

* To be finalized with members
Cu pillar CPI analysis on 28nm ELK and design optimization

**Multi-level CPI analysis and optimization**

- Flip chip process modeling analysis
  - Reflow process + capillary underfill
  - Thermo-compression + pre-applied underfill
- Package structural design analysis
  - Cu pillar design
    - Cu pillar structure
    - Dielectric materials
  - Substrate design and material
    - Core layer and BU layer
  - Underfill material
    - Cure dynamic
    - Material properties
- Comparison of impact of low-k, Ultra low-k (ULK) and Extreme low-k (ELK): parametric analysis of properties
- Novel flip chip design for next generation low K chip
  - Further analysis to identify important factors for further optimization

**Characterization and modeling analysis**

- Bump shear modeling: shear height to low K failure
- Perform bump shear testing with different shear height
- Numerical and experiment correlation
- Determine low K mechanical integrity

<table>
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<tr>
<th>Comparison of different method</th>
<th>Tensile Stress (Max)</th>
<th>Compressive Stress (Max)</th>
<th>Warpage</th>
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<tbody>
<tr>
<td>Normal Cu pillar bump after reflow</td>
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<td>TCNCP</td>
<td>0.70</td>
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<td>IME new design for next generation Low K chip</td>
<td>0.26</td>
<td>0.60</td>
<td>1.1</td>
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</tbody>
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(Source: IME)
Development and Characterization of ultra Fine Pitch Cu pillar interconnect on FC-CSP package test vehicle

Fabrication for ultra fine pitch Cu pillar and substrate

- Cu pillar of 30-20um pitch and 15-10um diameter *
  - High AR photoresist
  - Plating and bumping
  - Etching without undercut

- Fine pitch substrate
  - 2 layer organic substrate (30-20um pitch)*
  - Landing pad / lead sizes, shapes, surface finish
  - Si substrate for chip-chip attach (without TSV)

Process development and characterization of ultra fine pitch Cu pillar

- Thermo-compression with NUF, NCP, NCF*
- Exploration of solderless bonding for ultra fine pitch Cu pillar application

* To be finalized with members
Assembly Process development, Cu pillar Stress Characterization, Reliability Test and Failure Analysis

Assembly / process development of Cu pillar bumped 28nm Cu low K chip
- Pre-applied underfill material characterization
- Thermo-compression process characterization
- Bench mark with new design

Cu pillar stress characterization with sensor bumped chip
- Without underfill
  - Thermo-compression stress characterization
  - Reflow stress characterization
- With underfill
  - Thermo-compression with pre-applied underfill
  - Reflow + capillary underfill

Package assembly and reliability characterization
- Initial quick reliability assessment for design & material screening
- Final reliability assessment for final confirmation
- Reliability assessment and FA*
  - JEDEC standard testing: MST L3, TC, HTS test
  - Electromigration test

* To be finalized with members
Members inputs

- Finalize project scope / test vehicle spec
  - Cu pillar CPI analysis and design optimization
  - Test vehicle design & wafer fabrication
  - Fine pitch / low CTE substrate fabrication

- Experiment characterization
- Quick reliability assessment, material selection and improvement
- Reliability test vehicle fabrication
- Final reliability test and FA

Project Time line and schedule: Nov 2012 - April 2014 (18 months)
Possible Research Outcome

• **Cu pillar CPI analysis on 28nm ELK chip and design optimization**
  - Flip chip process analysis with capillary underfill and pre-applied underfill
  - Package structural design analysis and optimization
  - Novel design for next generation flip chip
  - Low K chip mechanical integrity characterization results

• **Development and Characterization with ultra Fine Pitch Cu pillar interconnect on FC-CSP package test vehicle**
  - Fabrication of ultra fine pitch Cu pillar and substrate
  - Process development and characterization of ultra fine pitch Cu pillar
  - EM modeling and characterization of ultra fine pitch Cu pillar

• **Assembly Process development, Cu pillar Stress Characterization, Reliability Test and Failure Analysis**
  - Assembly / process development of Cu pillar bumped 28nm Cu low K chip
  - Cu pillar stress characterization with sensor bumped chip
  - Package assembly and sample build for reliability characterization
  - Reliability assessment and Failure analysis
THANK YOU