Through-Silicon Interposer Technology for Heterogeneous Integration

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As 3D IC technology paves the way for future VLSI systems, it is also confronting bottlenecks such as tools for designing optimal 3D systems and thermal solutions for 3D ICs. Meanwhile, 2.5D through-silicon interposer (TSI) technology is also gaining momentum, both in the foundry and the outsourced semiconductor assembly and test (OSAT) universe.

A typical TSI is designed to host a set of guest dies interconnected to each other using the back end of line (BEOL) interconnects, while the through-silicon vias (TSVs) are leveraged to interface with the external I/O ports on the organic package and/or PCB. Backside RDL technology routing has a potential to track a likely good die (LGD) through testing. TSI technology not only provides easier fabrication capabilities, alleviating 3D thermal bottlenecks, it also supports the fabrication of high-performance heterogeneous integration.[1,2]

Versatile 2.5D Heterogeneous Logic + Memory System Design

Figure 1 shows a versatile 2.5D heterogeneous logic + memory system design. Ideally, the system should house a logic block integrated with high-speed memories supporting high-speed optical interface with the external world. Initial test vehicle simulation shows that on-chip interconnects provide more than 30x more bandwidth per watt compared with organic carrier. Moreover, the TSI reticle is large (2.67 x 4.3 cm²), and appears to be an ideal candidate for heterogeneous integration of the digital system. The large area of the TSI reticle is also instrumental in reducing the power density (W/cm²) constraint typically evident in real 3D stacked ICs.

Figure 1. Schematic of a versatile 2.5D Heterogeneous Logic + Memory System Design.

A future test vehicle, so-called “node” in the high-performance computing world, will be a complete system with an optical interface for the off-chip signaling. With such “nodes,” all on-chip data transfer is electrical with copper wires, while off-chip data transfer uses optical fiber interconnects to guarantee bandwidth and low-power operations. With such architecture, the main function of the TSVs is to provide power and ground (through a large array of TSV and BEOL power/grids) and a few I/O for the upper organic interconnect level such as a motherboard.

Such nodes or systems on TSI can operate in the Tbps regime (8xTbps) for on-chip data exchange. Bandwidth is transferred off-chip with single-mode fiber (SMF) optics at 1,550 nm optical wavelength, and optical bandwidth of 0.5 nm can carry 25 Gbps of data. For an SMF wavelength grid operating at 1,500–1,600 nm, it provides 5 Tbps per fiber or 10 Tbps in duplex mode.

Fabrication of TSI Interposer

A 300 mm Si-(100) substrate was used for TSI fabrication. The TSV was etched by a Bosch process after TSV lithography. Alternate deposition and etching achieved a 12 μm TSV with 100 μm depth. A 1 μm O3 TEOS with 1 kÅ PECVD SiO2 (field area)
was deposited after via patterning a TSV liner to isolate the TSV from the silicon substrate. Titanium and copper were sputtered on the TSV wafer as a barrier metal and copper seed. Copper void-free TSV was achieved by electroplating, and copper overburden was removed by a copper CMP process after copper annealing.

Three single-damascene processes were applied to form frontside (FS) M1, via and M2 on top of the TSV. The cross-section of TSV and FS metal is shown in the Figure 2 inset. Good connections are observed between TSV with M1 and M1-via-M2.

ZoneBOND technology[5] was used for wafer temporary bonding and de-bonding. TSV wafer was back-grinded near TSV depth before TSV exposed by the back-grinder. The remaining silicon substrate was etched to expose the TSV from the wafer backside (BS). Low-temperature dielectric films were deposited and a CMP process was applied for the planarization of BS dielectric films and TSV. BS barrier metal and copper seed were sputtered on the BS dielectric and TSV. BS RDL was patterned on barrier metal and copper seed. BS electroplating was used for the formation of BS RDL, and C4 bumps were built on top of the RDL. The final cross-section of interconnect is shown in Figure 2 after BS photoresist strip and barrier layer and copper seed etch back. Full connection between TSV, BS RDL and FS metals is shown in the Figure 2 inset.

**TSI Electrical Characterization**

The electrical performance of the TSI was characterized by an Agilent B1500A semiconductor device analyzer. C-V and i-V curves were characterized for TSV capacitance ($C_{TSV}$) and leakage current after top M2 metallization and before TSV revealing, treating measurement chuck as ground contact. The probability plots of the characterized TSV capacitance and leakage current are shown in Figure 3. $C_{TSV}$ characterization was performed at 10 kHz, 100 kHz and 1 MHz frequency to observe the $C_{TSV}$ variation in the low-
and mid-frequency range. The results are shown in the inset of Figure 3a. The accumulation and depletion capacitance of single TSV is ~300 and 180 fF respectively for a 12 μm TSV with 100 μm depth, and is in sync with the estimated average oxide liner thickness of ~420 nm.

$C_{TSV}$ response with applied voltage at different frequencies matches with theoretical description on the TSV capacitor. [6] The TSV processing yield is observed to be ~90%. Further, TSV leakage currents are characterized for the successful dies. The leakage between four TSVs with connection pad to silicon substrate (measured TSV good dies after C-V characterization) is less than 1 pA for a voltage range 0–100 V as shown in the inset of Figure 3b. The probability plot for the TSV leakage (Figure 3b) shows <1 pA leakage current and higher breakdown voltage >100 V for all TSVs, suggesting satisfactory isolation between the TSV and the silicon substrate.

TSV chain and BS RDL were characterized by four-points measurement on the first wafer after BS RDL. Figure 4 shows the results. The FS M1-TSV-BS RDL chain and FS M2-via-M1-TSV-BS RDL chain were characterized, with the results shown in Figure 4a. I-V curves of via chains ($R = R_{TSV} + R_{top\ metal} + R_{bottom\ metal} + R_{contact}$) were characterized, and are shown in the inset of Figure 4a. The yield of the FS M1-TSV-BS RDL chain and FS M2-via-M1-TSV-BS RDL chain are observed to be 90% and 85%, respectively, after the BS RDL process that is shown in Figure 4a. More process optimization is being investigated to improve the TSV yield further.

Four-points testing was applied to characterize the resistance of BS RDL (line/space 10/10 μm) and shown in Figure 4b. BS RDL performance shows a good I-V curve, as seen in the inset of Figure 4b. The probability plot (Figure 4b) shows a 100% electrical yield of BS RDL.

TSV integrated with FS four metal layers on 300 mm silicon substrate completed FS process development and electrical characterization. The wafers are processing BS metallization. The results will be reported in the future.

**Summary**

In this article, we demonstrated and characterized the TSI (with FS two metals and BS one metal) for heterogeneous integration. The preliminary electrical yield of the FS M1-TSV-BS RDL chain and FS M2-via-M1-TSV-BS RDL chain are 90% and 85%, respectively, on the first wafer. Ongoing processing improvements are in place to take yields to the high 90s.

The TSI platform offered at the Institute of Microelectronics (IME) is targeted for both low-cost and high-performance applications. In addition, IME offers multi-project wafer (MPW) services that allow our industry/research partners to prototype 2.5D ICs by using IME’s TSI fabrication and assembly/packaging capabilities.

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**References**


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