High RF Performance TSV Silicon Carrier for High Frequency Application

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Abstract

Three dimensional system-in-package (3D SiP) based on silicon carriers or interposer is a fast emerging technology that offers system design flexibility and integration of heterogeneous technologies. One of the key technologies enabler for silicon carrier is through silicon via (TSV). The development of 3D SiP will require the devices with different functionality operating at high frequency to be densely packed on the silicon substrate. However, silicon substrate is usually of low resistivity, when a high frequency signal is transmitted vertically through the substrate via, significant signal attenuation can occur that leads to poor RF performance. In this paper, a coaxial TSV structure in silicon carrier is presented for high frequency applications. The coaxial TSV is able to suppress undesirable substrate loss as well as provide good impedance matching. Electrical modeling of coaxial TSV structure was carried out to obtain the required geometries for impedance matching. Three different types of test vehicles were fabricated; Cu-plug TSV in both low (~10 Ω·cm) and high resistivity (~4000 Ω·cm) silicon substrate, and coaxial TSV in low resistivity silicon substrate. The S-parameters of the via structure of the test vehicles were measured from 100 MHz to 10 GHz. The measured results show that the coaxial TSV structure is able to suppress silicon substrate loss and provide good RF performance compared to Cu-plug TSV structure.

1. Introduction

Three dimensional system-in-package (3D SiP) is an advance packaging solution that enables interconnection between integrated circuits and other devices at high density far beyond those of current first-level packaging.

3D SiP development employing stacked silicon carriers is a fast emerging technology. Silicon carrier utilizes fine pitch back end of the line (BEOL) Cu wiring, high density solder interconnects and vertical through silicon vias (TSV). Silicon carrier technology allows modular chip design flexibility as well as ability to integrate heterogeneous technologies with performance comparable to or exceeding that of single chip integration [1-2]. The identical coefficient of thermal expansion of the silicon carrier and silicon chip also help to improve package reliability. In addition, passive circuits such as capacitor and inductors can be also embedded in the silicon carrier.

The development of SiP will require densely-packed devices with different functionalities such as integrated circuits and RF/microwave modules operating at high frequency. Silicon carrier is typically silicon having low resistance of 5-10 Ω·cm. The low resistivity silicon (LRS) substrate is well suited for the fabrication of CMOS and bipolar devices. However, when high frequency signals are transmitted vertically through the silicon substrate, the low resistivity proves to be very lossy. This results in significant signal attenuation leading to poor RF performance. Substrate loss will become a significant barrier toward the enabling of silicon carrier based 3D SiP. Several methods used to suppress substrate loss include the use of high resistivity (HRS) substrate [3-4] and thick insulating dielectric such as oxidized porous silicon [5-6]. However, high resistivity silicon substrate is costly and increases the cost of package. The use of thick oxidized porous silicon sidewall via can reduce substrate loss, but impedance mismatch between transmission line and TSV interconnects can lead to degradation of RF performance [6].

In this paper, a coaxial TSV structure was proposed to enable low resistivity silicon carrier based 3D SiP for high frequency application. The coaxial TSV structure offers complete shielding, which help to suppresses undesirable substrate loss. The coaxial TSV also allows controlled impedance matching for RF/microwave systems to achieve excellent RF performance.

2. Design of Coaxial TSV Structure

The structure of the coaxial TSV is shown in Fig. 1. The coaxial TSV consists of a silicon substrate through wafer via-hole with insulation barrier formed on the substrate and via sidewall. A conductive ground metallization layer is formed over the insulation liner with a thick layer of dielectric deposited inside the via-hole. At the center of the dielectric is a signal core. Transmission lines can then be formed to connect devices signal to the signal core.

![Fig. 1 Illustration of 3D SiP based on silicon carrier with coaxial TSV.](image-url)
3. Design for Electrical Performance

Electrical modeling was performed using Ansoft’s High Frequency Structure Simulation (HFSS) to study the signal propagation loss of the TSV structure. The frequency evaluated ranged from 100 MHz to 10 GHz.

For the coaxial TSV structure, the following parameters were varied to evaluate the signal propagation loss as well as to obtain the dimensions required to achieve good impedance matching: 1) dielectric constant, $K$, of the dielectric; 2) ratio of inner diameter of annular Cu ground plane, to the diameter of Cu signal core, denoted as $n$; and 3) thickness of the silicon carrier.

Fig. 2 shows the coaxial TSV model established in HFSS. The model consists of a coaxial TSV structure with a via-hole diameter of 300 µm created on a 1 x 1 mm² low resistivity (10 Ω cm) silicon substrate. The thickness of the Cu ground plane is fixed as 1 µm and the thickness of silicon oxide and silicon nitride is fixed as 1 µm and 100 nm, respectively. The Cu signal core is connected by 50 Ω microstrip transmission lines to the excitation wave ports.

The characteristic impedance of the coaxial TSV structure can be changed by varying the diameter ratio, $n$ and dielectric constant. Fig. 4 shows the transmission coefficient, $S_{21}$ at 10 GHz against diameter ratio, $n$ for different dielectric constant, $K$. The silicon carrier thickness was fixed as 300 µm. From the simulation result, the diameter ratio, $n$ required for good impedance matching (i.e. maximum $S_{21}$) varies for each dielectric constant, $K$. By decreasing the dielectric constant, $K$, the diameter ratio, $n$ required for good impedance matching decreases. The simulation also shows that a thick dielectric is required for the coaxial TSV to achieve good impedance matching and this restricts the dielectric materials that can be used, since not all dielectric materials can be deposited with high thickness along the via sidewall.

The coaxial TSV also has the potential of achieving a transmission coefficient, $S_{21}$ of greater than -0.5 dB at 10 GHz, showing that RF signal can be well transmitted with minimum losses.

The electric field distribution within the coaxial TSV is shown in Fig. 3. The electric field is confined within the via between the Cu ground plane and Cu signal core thereby resulting in less electric field energy loss to the substrate and help to suppress electrical coupling between adjacent vias.
Fig. 5 shows the transmission coefficient, $S_{21}$, at 10 GHz against $n$ for different silicon thickness with a fixed dielectric constant, $K$ of 3. Simulation results show that for the same diameter ratio, $n$, a reduction in the silicon carrier thickness increases the transmission coefficient. The RF performance of the package can be improved by employing a thinner silicon carrier with shorter electrical paths.

Based on the results from the electrical performance modeling, the following dimensions were selected for coaxial TSV structure test vehicle fabrication as shown in Fig. 1. The via-holes diameter is 300 $\mu$m and the silicon carrier thickness is 300 $\mu$m. The thickness of the Cu ground plane metallization is 1 $\mu$m.

A negative tone photoresist, SU-8 is selected for the dielectric material, since SU-8 is capable of developing high aspect ratio features [7]. In addition, SU-8 has good mechanical properties and can be retained as a final component of the finished structure as a dielectric material. SU-8 is reported to have a dielectric constant value of 3.25 and a loss tangent value of 0.035 [8]. Using these values in the electrical modeling, a radius ratio, $n$ of 3 is required to achieve good impedance matching, which means a 100 $\mu$m diameter Cu signal core need be filled at the center of the SU-8 dielectric for a 300 $\mu$m diameter via-hole.

Fig. 6 shows the Cu-plug TSV model established in HFSS. A ground-signal-ground via configuration is used to evaluate the transmission signal loss of the Cu-plug TSV. Via with a diameter of 300 $\mu$m and 500 $\mu$m pitch were created in a 5 x 5 mm$^2$ silicon substrate. The thickness of silicon oxide and silicon nitride is fixed as 1 $\mu$m and 100 nm, respectively. The ground vias are connected by a ground pad and annular excitation lumped ports are used to connect the ground pad to the signal via.

4. Test Vehicle Fabrication

Three types of test vehicles were fabricated; Cu-plug TSV structure in both LRS (~10 $\Omega\cdot$cm) and HRS (~4000 $\Omega\cdot$cm) substrate, and coaxial TSV structure in LRS substrate. All test vehicles were fabricated on 200 mm wafers. The size of the silicon carrier is 13.5 x 13.5 mm$^2$ with a thickness of 300 $\mu$m. The via-holes diameter is 300 $\mu$m and the vias are arranged in 3 depopulated rows of 500 $\mu$m pitch as shown in Fig. 7. For the coaxial TSV structure, the signal core diameter is 100 $\mu$m.

Fig. 7 Via-holes layout on the silicon carrier.

Figs. 8 and 9 shows the fabrication process of the Cu-plug TSV and coaxial TSV test vehicle, respectively. The fabrication of TSV requires the formation of through wafer via-hole This is achieved by using deep reactive ion etching (DRIE) to form blind via followed by back-grinding process to form the through wafer via-hole. 4 $\mu$m mask oxide was deposited on the front side of silicon substrate with a thickness of 700 $\mu$m. DRIE uses a Bosch etch process which comprises of alternate etching (SF$_6$) and passivation (C$_4$F$_8$) steps to create blind via of 300 $\mu$m diameter with nearly vertical sidewall. The mask oxide was removed by buffered oxide etch (BOE) and the wafer was back-grinded to 300 $\mu$m to form through wafer via-holes.

The 1 $\mu$m silicon oxide and 100 nm silicon nitride was then deposited by plasma-enhanced chemical vapor deposition (PECVD) onto the substrate surface and via sidewall. The silicon oxide and nitride liner serve two purposes; to act as an electrical insulation between the Cu metallization and silicon substrate and as a barrier to Cu migration from Cu metallization to silicon substrate.

A bottom-up Cu electroplating approach was used to fill the via-holes in the silicon carrier. To perform bottom–up Cu electroplating, an additional 200 mm perforated handler wafer was used. The perforated handler wafer was e-beam evaporated with a Cu-seed layer on both sides and a 50 $\mu$m dry film photoresist was laminated on the front side with an edge bead ring formed by lithography. An additional Cu-seed layer was e-beam evaporated on the patterned dry-film photoresist and this forms a continuous conductive Cu-seed layer that is used for bottom-up electroplating.
Fig. 8 Process flow of Cu-plug TSV test vehicle. (a) Mask oxide deposition and patterning. (b) DRIE to form blind via. (c) Backgrind to form through wafer via-holes. (d) Insulation barrier deposition. (e) Dry film photoresist lamination and patterning. (f) Bond to perforated handler by thermo-compression. (g) Bottom-up cu electroplating. (h) De-bond carrier.

For the Cu-plug TSV test vehicles, 20 µm dry film photoresist was laminated onto the front side of the substrate and via-holes openings were patterned onto the dry film photoresist by lithography. The silicon carrier was then bonded to perforated handler wafer by thermo-compression with the dry film photoresist acting as a sacrificial bonding layer.

The bonded carrier was then loaded onto a wafer holder with multiple metal fingers in contact with the backside of the perforated carrier wafer. A dc current density of 10 mA/cm² was used throughout the electroplating process. After the via-holes were completely filled with Cu, the carriers were separated from the perforated handler wafer by stripping the dry film photoresist.

For the coaxial TSV structure test vehicle, two more additional process steps are required after the deposition of the insulation barrier; the formation of the ground plane metallization, and dielectric via-filling.

Fig. 9 Process flow of coaxial TSV test vehicle. (a) Mask oxide deposition and patterning. (b) DRIE to form blind via. (c) Backgrind to form through wafer via-holes. (d) Insulation barrier deposition. (e) Sputtering of ground plane metallization. (f) Attach release film on backside and screen print SU-8 photoresist. (g) Pre-bake, peel off release film and pattern SU-8 by lithography. (h) Dry film photoresist lamination and patterning. (i) Bond to perforated handler by thermo-compression. (j) Bottom-up cu electroplating. (k) De-bond carrier.

The ground plane was formed by sputtering a layer of 1000 Å of Ti and 1 µm of Cu onto the substrate surface and along
via sidewall. An additional 2000 Å of Cr was then sputtered on top of Cu to improve the adhesion of the SU-8 dielectric in the via-holes.

A release film was first attached to the backside of silicon carrier substrate and SU-8 was deposited by screen printing followed by pre-baking at 65°C for 15 minutes and 95°C for 50 minutes in an oven. After pre-baking, the release film was peeled off from the silicon carrier backside leaving the SU-8 photoresist in the via-holes. SU-8 photoresist was then patterned using lithography. The SU-8 dielectric was exposed to UV radiation at an intensity of 350 mJ/cm² and post exposure baked at 95°C for 15 minutes. SU-8 was developed using SU-8 developer and rinsed with iso-propanol to form the via-holes. Oxygen plasma was then used to remove any residue that remains in the via-holes.

20 µm dry film photoresist was laminated to both sides of the silicon carrier and via-holes openings were patterned onto the dry film photoresist by lithography. The silicon carrier was then bonded to the perforated hander wafer for bottom-up Cu electroplating in a similar manner as with the Cu-plug TSV test vehicle. A dc current density of 10 mA/cm² was used throughout the electroplating process. After the via-holes were completely filled with Cu, the carrier was separated from the perforated hander wafer by stripping the dry film photoresist.

Fig. 10 shows the optical images taken at different process steps during the fabrication of the coaxial TSV test vehicles. Fig. 11 shows the optical images of coaxial TSV and Cu-plug TSV structure fabricated on the silicon carrier.

![Image](image_url)

Fig. 10 Optical images during coaxial TSV process steps: (a) SU-8 photoresist via-filling after screen printing. (b) Via-hole developed in SU-8 photoresist. (c) Dry film photoresist lamination on substrate followed by thermo-compression to perforated carrier. (d) Via-hole filled with electroplated Cu after stripping dry film photoresist.

Fig. 12 (a) shows the SEM image of the cross-section of the coaxial TSV test vehicles. The through wafer via-holes were filled with SU-8 dielectric and the via-holes developed in SU-8 dielectric has nearly vertical sidewall. Cu was electroplated into the SU-8 via-holes with no voids. Fig 12 (b) shows the close up images of insulation barrier and ground plane metallization. The thickness of the insulation barrier and ground metallization along the via-sidewall was approximately 1 µm each. Fig. 13 shows the SEM image of the cross-section of the Cu-plug TSV test vehicles. Cu was electroplated into the via-holes with no-voids.

![Image](image_url)

Fig. 11 Optical image of (a) coaxial TSV structure, (b) Cu-plug TSV fabricated in silicon carrier taken from the front side.

![Image](image_url)

Fig. 12 (a) SEM image of cross-section of coaxial TSV structure, (b) Close up SEM image of the insulation barrier and ground plane metallization.
5. High frequency electrical characterization

To measure the S-parameters of the TSV structure, the test vehicles were bumped with 150 µm diameter eutectic SnPb solder balls and flip chip assembled on grounded-coplanar waveguide fabricated on Roger RO4035B high frequency board. Two ports measurements were performed using a vector network analyzer and cascade microwave ground-signal-ground probes (GSG). S-parameters were measured from 100 MHz to 10 GHz. The ground-signal-ground via structure is shown in Fig. 14. The test structure consists of 3 vias, with the center via acting as the signal via and the adjacent vias connected to the ground. For the coaxial via structure, an additional Cu probing pad was fabricated onto the silicon carrier to connect the two adjacent vias to the ground plane.

6. Measurement Results and Discussion

Fig. 15 shows the measured and simulated S-parameters of the test vehicles after de-embedding. The solder bump interconnects were not included in de-embedding and so the actual transmission loss of the via will be lower than that of measured. Since the solder bump interconnects were not included into the electrical modeling, the measured transmission loss was higher than that of the simulated. Variation in the resistivity of the silicon substrates used in the fabrication could be another reason for the difference between the measured and simulated values.

Fig. 15 Measured and simulated S-parameters: (a) Transmission coefficient, S_{21}, (b) Reflection coefficient, S_{11}, for Cu-plug TSV in low resistivity silicon (LRS) and in high resistivity (HRS) silicon substrate, and coaxial TSV in low resistivity substrate.
From Fig. 15 (a), the measured transmission coefficient, $S_{21}$ at 10 GHz for Cu-plug TSV in HRS and LRS substrate are -1.53 dB and -4.96 dB, respectively. The high transmission loss in Cu-plug TSV in low resistivity silicon is mainly contributed by the substrate loss as well as impedance mismatch. By using a high resistivity silicon substrate, the transmission loss of the Cu-plug TSV structure can be reduced further by 3.43 dB at 10 GHz. For the coaxial TSV structure in low resistivity silicon substrate, the measured $S_{21}$ at 10 GHz is -0.33 dB, which shows the lower transmission loss than that of the Cu-plug TSV structure in both LRS and HRS.

Fig. 15 (b) shows the reflection coefficient, $S_{11}$ of the test vehicles. The measured $S_{11}$ at 10 GHz of the Cu-plug TSV structure in both HRS and LRS substrate are -12.39 dB and -12.09 dB, respectively. At 10 GHz, the difference in the resistivity of the silicon substrates does not have significant effect on the reflection loss in the Cu-plug TSV test vehicles. As for the coaxial TSV structure, the measured $S_{11}$ at 10 GHz is -16.41 dB, showing lower reflection loss as compared to Cu-plug TSV structure.

By employing the coaxial TSV structure in LRS substrate, the RF signal loss can be reduced significantly. This result shows that the coaxial via structure can effectively suppresses undesirable substrate loss and provides good impedance matching. This will enables the use of LRS substrate as silicon carrier for high frequency application.

7. Conclusions and Recommendations

A coaxial TSV structure for silicon carrier based 3D SiP has been developed for high frequency application. Electrical modeling was performed using Ansoft’s HFSS in order to obtain the required dimensions of the coaxial TSV structure for good impedance matching. Three different types of test vehicles were fabricated; Cu-plug TSV in both LRS (~10 Ω·cm) and HRS (~4000 Ω·cm) substrate, and coaxial TSV in LRS substrate. The S-parameters of the TSV structure of the test vehicles were measured from 100 MHz to 10 GHz. Some important results and recommendations are summarized in the followings.

1) Electrical modeling results showed that coaxial TSV is capable of suppressing undesirable substrate loss to a frequency of 10 GHz and also allows controlled impedance matching.

2) Fabrications process for both Cu-plug TSV and coaxial TSV structures in silicon carrier have been developed and test vehicles were fabricated.

3) The measured transmission coefficient, $S_{21}$ at 10 GHz for the coaxial TSV structure in LRS substrate, Cu-plug TSV in HRS and LRS substrate are -0.33 dB (the best), -1.53 dB and -4.96 dB, respectively. By employing the coaxial TSV structure, the transmission loss was reduced by 1.2 dB and 4.63 dB as compared to Cu-plug TSV structures in HRS and LRS structure at 10 GHz, respectively.

4) The measured reflection coefficient, $S_{11}$ at 10 GHz for the coaxial TSV structure in LRS substrate, Cu-plug TSV in HRS and LRS substrate are -16.41 dB (the best), -12.39 dB and -12.09 dB, respectively. By employing the coaxial TSV structure, the reflection loss was reduced by 4.02 dB and 4.32 dB as compared to Cu-plug TSV structures in HRS and LRS structure at 10 GHz, respectively.

5) Since the coaxial TSV structure exhibits excellent RF performance and enables the use of LRS substrate as silicon carrier for high frequency application, so the use of LRS substrate will help to reduce the cost of silicon carrier based 3D SiP as compared to utilizing costly HRS substrate.

Acknowledgments

The authors would like to thank the following colleagues at Institute of Microelectronics: Yang Riu N. Ranganathan, Liao Ebin, K. W. Teoh, W.S. Lee and Y.M. Khoo for their valuable support in this work.

References