Development of a Low Cost 2.5-Gbps SFP Optical Transceiver using 0.18µm CMOS ICs

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ABSTRACT

The high cost of optoelectronics components typically used for long-haul communication is prohibitive in the Fiber to the Home (FTTH) and Passive Optical Networks (PONs). One method of cost reduction is through reducing the cost of the electronics in the transceiver and reducing the packaging cost. We report the development of low-cost 2.5-Gbps optical transceiver for Gigabit Passive Optical Network (GPON) using CMOS driver ICs and chip-on-board assembly method. We developed the Laser Diode Driver (LDD), Trans-impedance Amplifier (TIA), Limiting Amplifier (LA) and the Clock and Data Recovery (CDR) using CMOS technology for short reach application and developed the burst mode version of the ICs for PON applications. The ICs are designed in house and fabricated on a standard CMOS 8” wafer with 0.18µm technology. The devices operate at 1.8V and are low power in nature, thus reducing the demand on power dissipation. The transceiver consists of an un-cooled and direct modulated laser diode driven with a LDD, a high speed PIN photo-diode with amplifier and CMOS ICs. The bare CMOS ICs are attached on a transceiver substrate that is compliant with the small form-factor pluggable (SFP) package multisource agreement (MSA) and coupled to a 1310nm FP laser TOSA and a PIN ROSA with LC connector. The integrated transceiver is characterized up to 2.5-Gbps. In this publication, we present the detail of the module development, assembly methods and performance characterization at 1310nm.

Keywords: 2.5-Gbps SFP, optical transceiver, 0.18µm CMOS technology, FTTH, GPON

1. INTRODUCTION

With increased in demand for faster applications such as data transfer and video, the IP traffic grew rapidly. This stimulated the development of low-cost and high performance optical access network. Passive Optical Network (PON) is one of the emerging cost-effective and high-performance methodologies to be looked into for the last mile communication. A typical PON consists of the Optical Line Terminal (OLT) located at the Central Office (CO) that is responsible for broadcasting information downstream to the users through an Optical Network Unit (ONU). Information is transmitted upstream from the users, superimposed at combiner and sent to the OLT at the CO. The data from the users must be buffered and transmitted in short burst to avoid collision. The CO will decide which user to send a burst at which point in time, thus upstream traffic flow, shown in Figure 1a, requires burst-mode transmission.
In the downstream traffic, Figure 1b, the OLT will tag the data with addresses and broadcast it to all the users sequentially. Each user will merely select the data that has the appropriate address tag; therefore, conventional continuous transmission can be exploited.

This paper looks into the development of a 2.5-Gbps optical transceiver for short reach application for G-PON (Gigabit Passive Network) using 0.18μm CMOS ICs. To achieve low-cost in the GPON transceiver development, one method is to reduce the cost of the electronics in the transceiver by going for CMOS ICs. On top of that, packaging cost of ICs can be further reduced by using direct chip-on-board assembly method. The CMOS ICs are integrated onto the small form factor transceiver. Over the years, there are quite a few research developments on ICs using 0.18μm CMOS technology [1][2][3] to drive optoelectronics components. However, their experiment focuses on either the receiver or the transmitter. The evaluation for CMOS IC transceivers has not been extensively carried out. Section II gives details of the design configuration and circuitry of the transceiver module. Assembly and the transceiver characterization methodology will be described in detail in Section III. Transceiver test results are presented in Section IV. Last but not least, conclusion is covered in Section V.
2. TRANSCEIVER DESIGN CONFIGURATION

The block diagram of the transceiver block is illustrated in Figure 2. It is sub-divided into optical and electrical block. The optical block consists of a transmitter optical sub-assembly (TOSA) and a receiver optical subassembly (ROSA). The commercial un-cooled Fabry Perot (FP) TOSA is a multi-rate 1310nm direct modulated source laser that is packaged within an LC receptacled transmitter optical sub-assembly. The commercial receiver optical sub-assembly (ROSA) integrates a 2.5-Gbps PIN Photodiode and a low noise trans-impedance amplifier (TIA) into a hermetic TO stem. The PIN is composed of an InGaAs absorption layer, thus it is suitable for 1310-nm applications.

The electrical block is further divided into 2 subsections, namely the transmitter and the receiver sections. The transmitter portion contains a laser diode driver (LDD) that is developed using 0.18µm CMOS technology. The LDD requires a 1.8V and 3.3V supply voltage. It can modulate laser diodes up to 20mA and can supply bias current up to 30mA. The LDD is designed to operate up to 2.5-Gbps; with a rise and fall time of about 180ps. The achievable extinction ratio with this driver is 8dB. The LDD can function in both continuous burst mode, simply by varying the input level at burst enable control pins $BEN^+$ and $BEN^-$. By supplying a 1.8V to the $BEN^+$ pin and connecting the $BEN^-$ pin to ground, the laser driver will function in continuous mode. Conversely, by applying a burst enable signal to the $BEN^+$ and $BEN^-$ pins and some additional circuitry, the LDD will then operate in burst mode. The receiver section is composed of a limiting amplifier (LA), as illustrated in Figure 4. It is the stage following TIA, which further amplifies voltage signal and generates constant output level. The amplifier has bandwidth of more than 2.5-Gbps and accepts input range from 50mV to a maximum of 250mV. It provides constant current-level current-mode logic (CML) output voltages of about 200mV.

In this work, we use the package type which is compliant with SFP package. This package has a very small physical dimension and it is hot-pluggable, thus enables easy testing via host boards without having to turn off the DC bias [4]. The SFP transceiver is designed on a 4-layer FR4 material with board thickness of about 1mm. Split power DC power planes is implemented for transmitter and receiver to prevent any crosstalk. The transceiver module is targeted to operate up to 2.5-Gbps.

Fig. 2. Transceiver module
3. TRANSCIEVER ASSEMBLY AND CHARACTERIZATION

In order to eliminate the parasitic effects of the through-hole connections which will degrade the performance of the transceiver, the TOSA and ROSA are both edge mounted onto the SFP substrate. The laser driver and the limiting amplifier are assembled and connected to the transceiver substrate using chip-on-board (COB) method to further reduce the parasitic effects introduced by leads of packages, in addition to the reduced cost due to the elimination of packaging cost. The CMOS driver ICs are firstly wire-bonded onto the PCB board before the rest of the passive components are reflow soldered onto the same board. A high purity liquid epoxy encapsulant used as glob top is applied onto the wire-bonded driver ICs and cured in order to protect the bond wires during the high reflow temperature and handling during characterization.

Transmitter testing is carried out by injecting a pseudo-random bit stream (PRBS), non-return-to-zero (NRZ) 2\textsuperscript{15}-1 patterns into the input of the CMOS laser diode driver, through the host board. The optical output from the TOSA is...
directly connected, via single-mode fiber, to a digital sampling oscilloscope optical module where the eye diagram is captured and measured.

Fig. 6. Transmitter test set up

For the receiver testing as shown in Figure 7, a reference transmitter is used as the source to send PRBS signal to the receiver. The reference transmitter optical signal, as shown in Figure 7, has an extinction ratio of about 10dB, optical power of -5dBm and a rise/fall time of around 180/200ps. The receiver under test consists of a PIN photodiode and a trans-impedance amplifier integrated in a commercial ROSA and a CMOS limiting amplifier. The PIN photodiode converts the optical signal into electrical current while the trans-impedance is responsible for converting the photodiode current into voltage with some amplification. The limiting amplifier further amplifies the electrical signal. The reference optical signal is transmitted through a singlemode fiber and received at the receiver under test.

Fig. 7. Receiver test setup using a reference transmitter
4. RESULTS

Characterization of the SFP transceiver is performed up to 2.488-Gbps. Optical power of -2dBm is attained and the extinction ratio is 8dB. The extinction ratio can be fine-tuned by adjusting the biasing and modulating current, which are controlled by the SMT trimmers assembled on the SFP transceiver. Some overshoot and undershoot are observed at the optical eye. This phenomenon can be improved by selection of appropriate damping resistor on the SFP, connected at the cathode of the laser diode. Alternatively, an RC shunt network consisting of a resistor and a capacitor connected to between the laser diode and the laser driver can be fine tuned to further improve the ringing or overshooting. The presence of lead and bond wires length that introduces parasitic inductance which may be the cause for the overshoot observed in the eye diagram. More significant jitter can be observed when the bit rate is increased from 1.244-Gbps to 2.488-Gbps. The summary of the transmitter is shown in Table 1(a).

Fig. 8. Reference transmitter eye diagram at 2.488-Gbps

Fig. 9. Optical eye diagram at 1.244-Gbps
Table 1 (a) Transmitter measurements using 1310nm Fabry Perot laser diode (b) Receiver measurements using 1310nm PIN photodiode, with the reference transmitter.
It is observed that zero crossings of the recovered electrical eye diagram at 2.488-Gbps is shifted above the midpoint. Possible causes of the above phenomenon could be due to differences in the current paths during the rise and fall time. This happens because each path may present distinct charging/discharging characteristics. Possible solutions could be to select a proper damping resistor that is connected between the laser diode cathode and the LDD. Nevertheless, the eye diagram is wide and clean from jitters, even at 2.488-Gbps.

Figure 13 shows the BER characteristics of optical the transceiver. A variable optical attenuator (VOA) is connected between the reference transmitter source with output optical power of -5dBm and the receiver under test. The VOA is adjusted to vary the optical signal received at the receiver and the recovered electrical eye and BER is measured at the sampling oscilloscope and Anritsu BERT scope respectively. It is found that the BER at -23dBm and -22dBm of received optical power are $10^{-11}$ and $10^{-9}$ respectively at 1.244-Gbps. Therefore, we conclude that the receiver sensitivity at 1.244-Gbps is -23dBm. A summary of the characteristics of the receiver is shown in Table 1(b).
5. CONCLUSIONS

This work demonstrates the integration of 0.18um chip on board CMOS ICs on standard SFP transceiver to attain a low cost optical transceiver that is targeted to operate up to 2.5-Gbps. The transceiver exploited the due to its small size and hot-pluggable feature. The transmitter is able to output around -2dBm of optical power and achieving up to 8dB extinction ratio at room temperature. The receiver has proven to achieve a sensitivity of -22dBm with BER $10^{-11}$. Further work is being carried out for future developments on the burst-mode features of the CMOS ICs.

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Fig. 13. Receiver sensitivity at 1.244-Gbps