Charge-Based Capacitance Measurement Technique for Nanoscale Devices: Accuracy Assessment Based on TCAD Simulations

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Abstract—In this brief, we carried out extensive mixed device and circuit-mode simulations to calibrate the charge-based capacitance measurement technique specifically for subfemtofarad nanowire-based device capacitance. The factors that influence the accuracy of the technique were identified.

Index Terms—Charge-based capacitance measurement (CBCM) technique, nanoscale devices, nanowire MOSFETs, sub-femtofarad capacitance measurements, transient TCAD simulations.

I. INTRODUCTION

MooRE’S law has dictated continuous decrease in the feature size of the CMOS devices which makes the short channel effects almost insurmountable for bulk CMOS technology. Device scaling is, thus, poised to usher into nanoscale with the emergence of novel device structures. These nanoscale devices, such as FinFETs and nanotube FETs, are besetted with the problem that a large area capacitor similar to that in the bulk CMOS technology is not available for characterization of the charge of channel carriers. As the capacitance of a single channel device falls far below the measurement range of conventional ac-bridge-based instruments, many investigators connect hundreds of devices in parallel to bring the collective capacitance to a measurable level. This is undesirable because the inherent variation, a characteristic of all nanoscale structures, gets eclipsed. Charge-based capacitance measurement (CBCM) technique, proposed for measuring the interconnect capacitance with small magnitude [1], also emerges as a promising technique for measuring low capacitance of active devices [2] and may have the potential of accurate capacitance measurement of single channel device. However, there are hardly any reports [3] in the literature assessing the accuracy of this technique and the parameters influencing it. In this brief, we investigate the accuracy of the technique with mixed-mode TCAD simulations and identify the factors that influence it.

II. PRINCIPLE OF CBCM

Fig. 1(a) shows the principle of capacitance measurement using CBCM: two drivers—one PMOS and the other NMOS form a pseudoinverter. By switching the two drivers “on” and “off” alternately, the load capacitance comprising the capacitance of Device Under Test (DUT) and parasitic capacitance is charged to \( V_{DD} \) when PMOS is turned “on” and discharges to ground \((V_{SS})\) when NMOS is turned “on.” The capacitance presented at the drain node of the pseudoinverter [depicted by “X” in Fig. 1(a)] is obtained from \( Q_{V_{DD}} \) which is found by integrating the charging current \( I_{V_{DD}} \) over one pulse period, or \( 1/f \) as in

\[
Q_{V_{DD}} = \int_{0}^{f} (C_{DUT} + C_{par})dV = \int_{0}^{1/f} I_{V_{DD}}dt.
\]

Another charging current \( I'_{V_{DD}} \) which charges only the parasitic capacitances can then be obtained by repeating the measurement on a structure without the DUT [1], or, by applying a third nonoverlapping pulse to the source and drain of the DUT during the measurement [2], as an additional step.

As shown in Fig. 1(b), the nonoverlapping pulse applied to DUT source and drain brings the voltage at this terminal to \( V_{DD} \) or \( V_{SS} \) to which the node X will be charged when the respective drivers (N or P) get turned on. Thus, no net charge gets stored on the DUT capacitance and DUT remains “invisible” when the pulses PG (or NG) and DUT S/D reach their flat portions. Small signal capacitance \( C_{DUT} \) can be calculated by differentiating the difference of the two measured currents, namely, \( I_{V_{DD}} \) and \( I'_{V_{DD}} \), are given by

\[
C_{DUT} = \frac{d(Q_{V_{DD}} - Q'_{V_{DD}})}{dV_{DD}} = \frac{d(I_{V_{DD}} - I'_{V_{DD}})}{dV_{DD}} \cdot \frac{1}{f}.
\]

We investigate the accuracy of the technique with the help of careful TCAD simulations using MEDICI. The capacitance predicted by MEDICI using small signal analysis is taken as reference.
Fig. 1. (a) Test-key circuit schematic for CBCM. (b) Input pulses for terminals NG, PG, S and D, dashed horizontal line indicates the constant voltage applied to S and D in order to scan the effective $V_{gs}$ for both polarities. $V_x$ shows the voltage response at the node “X,” or the gate terminal of the DUT, when the nonoverlapping pulse is applied to terminals S and D. It also shows the transient currents $I_{VDD}$ and $I'_{VDD}$ measured from the terminal VDD. $V_{DD}$ and $V_{SS}$ levels are labeled on DUT S/D pulse. Higher levels of NG and PG pulses ensure that the drivers are fully turned “ON” and “OFF.”

III. SIMULATION SETUP

The schematic of the simulated circuit is shown in Fig. 1(a). The DUT is a gate-all-around device that has a gate length of 0.25 $\mu$m and a cylindrical diameter of 10 nm. In order to simulate DUTs comprising multiple fingers, the “WIDTH” parameter in MEDICI was used as a multiplicity factor to account for the number of nanowires connected in parallel. The main advantage of using a physical DUT device is that it will automatically account for all the physics of the charge movement including nonquasi-static effect, if any. Modified Local Density Approximation Quantum Model in MEDICI was used to account for the quantum–mechanical effects in our DUT structures. On the other hand, drivers which essentially function as switches with attached junction and overlap capacitances are emulated by compact models (BSIM3 version 3.2, level 49 in MEDICI mixed-mode simulation). This setup captures the nanoscale DUT physically while ensuring proper convergence and economizing the computational resources. All compact model drivers have gate length of 0.18 $\mu$m and width of 0.5 $\mu$m.

The pulse repetition frequency is 45 MHz. Change in frequency has no significant effect on results. Furthermore, we optimized the time step in these transient simulations minimizing the inaccuracy introduced by simulation itself (equivalent to enhancing accuracy in current measurement). We have chosen the charge injection-free method [4] of capacitance measurement as it claims to be more accurate than others, although our evaluation method can be adapted to other variants of technique without exception. The transient currents obtained from the simulation are integrated numerically over one pulse period to obtain the charge used in (1) and (2).

IV. SOURCES OF ERROR AND EFFICACY EVALUATION

The main source of error in the technique is the charge injection through $C_{gs}/C_{gd}$ of drivers during the switching-off process. The amount of charge injected to $V_{DD}$ depends on the rise/fall times of the pulses, magnitude of the $C_{gs}$ or $C_{gd}$, and also on the magnitude of capacitance of the DUT $C_{DUT}$. This is clearly shown in Fig. 2, where $C_{par}$, obtained by differentiating charging current $I'_{VDD}$ for 100-finger and single-finger DUT, are compared with the parasitic capacitance given by the compact model (BSIM3) of the driver devices. It is worth noting here that although the DUT is supposed to be “invisible” during measurement of current $I_{VDD}$, its source/drain terminals have been precharged to the same voltage as that at node X, its presence still affects the charge injection. This is because during the transition period in which the drivers are being turned on or off, the net voltage between DUT gate (node X) and S/D terminals is nonzero and varies with time. The displacement current ($C \frac{dV}{dt}$) influences the charge flowing from/to $V_{DD}$ ($V_{SS}$). Therefore, $C_{DUT}$ still plays a role in deciding the amount of charge injected to $V_{DD}$. This is shown in the inset to Fig. 2 which shows a clear difference in magnitude of
time-dependent currents \( I'_{DD} \) for 100-finger and 1-finger devices and explains the difference in the parasitic calculations from BSIM3 models and CBCM computations as well as the difference between parasitic computed for 100-finger and 1-finger DUTs with the same set of drivers. On the other hand, for extraction of capacitance of DUT, we find that the impact of charge injection is significantly reduced through cancellation from BSIM3 models and CBCM computations as well as vices and explains the difference in the parasitic calculations.

The second source of error is introduced by the numerical evaluation of the capacitance using (2). The numerical inaccuracy becomes particularly prominent when the DUT capacitances become comparable to or lower than the parasitic capacitance presented by the pseudoinverters. For very small DUT, charging currents \( I_{DD} \) and \( I'_{DD} \) become very close in magnitude; therefore, any error in current gets amplified during subtraction and differentiation, resulting in noisy \( C_{DUT} \) curves. The numerical error in differentiation can be corrected by following Savitzky and Golay’s (S-G) algorithm [5]. As shown in Fig. 2, the noise in \( C_{par} \) is reduced substantially using S-G differentiation algorithm as compared with conventional finite difference (FD) method.

The simulation results in terms of per finger capacitance for DUTs having different number of fingers are shown in Fig. 3 and are compared with the capacitance obtained from small signal analysis in MEDICI using signal level of \((kT/10q)\) and frequency: 1 MHz. It can be seen that the \( C_{DUT} \) simulated by CBCM is smoother with higher number of fingers in the DUT, i.e., higher total DUT capacitance value. Comparing the two curves for 5-finger DUT using FD method and S-G method, it is clear that S-G algorithm effectively reduces the fluctuations and obtains smooth \( C-V \) curves. If S-G algorithm is properly applied, even single-finger DUT device whose magnitude is less than 380 aF can be extracted/measured with reasonable accuracy.

V. LIMITS OF CBCM TECHNIQUE

In order to properly design the CBCM test-key, it is important to understand the lower limit of the CBCM method and the factors affecting it. Although, as previously mentioned, the frequency of the pulses should not affect the extracted result of \( C_{DUT} \) if both the parasitic and DUT capacitances are very small, \( I_{DD} \) and \( I'_{DD} \) might both be too low to be assessed accurately. This will cause error in the extracted DUT capacitance on the account of degraded accuracy of the measured current. In such cases, increasing the pulse repetition frequency will increase the current through \( V_{DD} \) and, in turn, improve the accuracy of the technique. In terms of test-key design, the most important factor is the ratio of \( C_{DUT} \) with respect to \( C_{par} \). We plot the rms error in CBCM capacitance against the ratio \( C_{DUT}/C_{par} \) in Fig. 4. For \( C_{DUT} \) values less than half the \( C_{par} \) values, the error is less than 5% using FD method and improves to 3% using S-G algorithm. The rms error increases rapidly as the value of \( C_{DUT} \) falls below 20% of \( C_{par} \) as shown in the inset of Fig. 4—the error increases by more than 10% for each 5% increase in \( C_{par} \). The simulations bring out the fact that the parasitic capacitance due to the drivers of pseudoinverters and interconnects should be less than twice the minimum capacitance to be measured using CBCM to ensure the measurement accuracy of better than 5%.

VI. CONCLUSION

In this brief, we evaluate the CBCM technique in detail for subfemtofarad voltage-dependent capacitance measurement using intensive mixed-mode TCAD simulations. The effects of charge injection and numerical error are delineated. Practical design guidelines are arrived at for the desirable relative size of \( C_{par} \) and \( C_{DUT} \). Noise-free differentiation scheme proposed by S-G was found to give more accurate and smooth derivatives for CBCM capacitance extraction.

REFERENCES


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