In this work, we demonstrate for the first time, the successful integration of pure Ge S/D stressors (with low Ge %) in multiple-gate transistors [1],[2]. Integrating embedded SiGe stressors with Ultra-Thin Body (UTB) SOI planar or even nanowire transistors is extremely challenging, since there is very limited margin for Si/Ge excess prior to SiGe epitaxy. With reduced body thickness, lattice strain coupling from the S/D stressors is reduced. No successful attempt has ever been reported on forming Ge S/D stressors or even embedding Ge S/D stressors in nanowire-FETs or UTB-FETs.

In this work, we demonstrate for the first time, the successful integration of pure Ge S/D stressors with planar UTB-FETs and nanowire-FETs, resulting in very dramatic performance enhancement. The effect of substrate compliance in reducing defect density and increasing induced channel strain is also exploited. We further show that such highly-strained Ge S/D devices can be further improved by employing a laser-free MeltED diffusion and activation technique which uniformly dopes the Ge S/D regions. This technique simultaneously forms embedded SiGe stressors with very high Ge content (up to ~85%), effectuating further strain-induced hole mobility enhancement as a result of improved lattice strain coupling.

Device Fabrication

Multiple-gate ultra-thin body transistors with 30-80 nm widths were fabricated on 8 mm thick (100) surface Si wafers. Fig. 1 summarizes the key process steps. The gate etch process was tuned to produce bottom-tapered gates for small physical channel lengths. A translucent bottom-tapered gate running over a nanowire is shown in Fig. 2a), the gate length of which is obtained from TEM to be 5 nm. To induce high compressive channel strain, lattice-mismatched Ge stressors were epitaxially grown in the S/D regions of 3 device splits. Selectivity of the gate was achieved over SiOₓ and SiN, as shown in Fig. 3.

Two of these device splits have thick Ge S/D stressors: ‘Thick Ge S/D’, which is unembedded, and ‘Ge S/D (MeltED)’ which is embedded with a new Laser-Free Melt-Enhanced Dopant (MeltED) Diffusion and Activation Technique to be described later. One split (‘Thin Ge S/D’) has a thin Ge S/D stressor; the thickness of which is 50% that of the other two splits. For the splits with thick Ge stressors, one split (Ge S/D (MeltED)) was capped with SiOₓ and subjected to a 950°C RTA during S/D activation. This melted the Ge film which immediately re-crystallized upon cooling, using the underlying Si as a seed. The other two Ge splits and the Si control were also capped with SiOₓ but underwent a non-melt 900°C RTA during S/D activation.

Results and Discussion

A. Ge S/D stressor technology for UTB planar and nanowire transistors

Ge S/D stressors (Thick Ge) result in 80% Iₓxx enhancement (Fig. 4) and 135% Iᵧᵧᵧ enhancement (Fig. 5) over Control devices with raised Si S/D at a fixed Iᵧᵧᵧ of 1 x10¹⁷ A/m². Device width W is 80 nm. At a fixed DBL of 75 mN/mm, 105% enhancement in peak linear transconductance Gᵧᵧ is obtained. Such a large Gᵧᵧᵧ enhancement indicates large hole mobility enhancement due to compressive channel strain. Gᵧᵧᵧ enhancement is more pronounced at larger DBL values (shorter Lₑₑₑ), in agreement with typical observations for other local S/D stressor technologies. While Ge films more than a few nanometers thick tend to relax significantly when grown on bulk Si, substrate compliance in ultrathin Si SOI possibly allows for greater elastic strain accommodation due to the enhanced viscous flow of the underlying SiOₓ under large amounts of shear stress [3]. Furthermore, narrow structures tend to allow elastic lateral expansion of the Ge film [4]. TEM analyses (Fig. 7) showed that Ge grown on a wider SOI pattern had a much higher defect density compared to a narrower nanowire-like pattern, which has few observable defects. Fig. 8 shows the dependence of Iₓxx (extracted from Iᵧᵧᵧᵧ–Iₓxx plots) on device width. For the control device with raised Si S/D, the increase in Iₓxx with smaller W can be attributed to the non-negligible contribution of sidewall conduction in the 8 nm SOI. A trend of increasing strain-induced enhancement with decreasing W is observed. This correlates well with the reduced defect density in narrow patterns. For W = 30 nm, 96% Iₓxx enhancement was obtained for the Thick Ge S/D split, with the Thin Ge S/D split not too far behind (77%). This is especially significant, considering that the Thin Ge split only has half the Ge S/D stressor thickness. It also suggests that for devices with very narrow widths, e.g. nanowire devices, a thin Ge S/D stressor may be sufficient to induce large channel strain for significant performance benefits.

B. MeltED Diffusion and Activation Technique & Stressor Embedding

Key steps for forming MeltED or embedded Ge S/D stressors is shown in Fig. 9. When Ge is melted at temperatures exceeding 938°C, extremely fast liquid-state diffusion of dopants allows for rapid and uniform distribution of dopants throughout the Ge S/D stressor. During this process, Si and Ge inter-diffusion also occurs at the heterointerface, resulting in “embedding” of the Ge stressor for improved channel stress coupling effects. Fig. 10 shows the sheet resistance values of films with different Ge thicknesses. The films were doped near the surface with low energy 5keV BF²⁺ implantation of identical dose. After capping and undergoing the MeltED anneal, the sheet resistances were measured and plotted with calculated resistivity values in Fig. 10. The identical resistivity values clearly indicate uniform distribution and incorporation of B in Ge. Hence, the results prove that this technique can facilitate uniform dopant diffusion and incorporation regardless of Ge thickness or S/D geometry.

Compared to Ge S/D devices without Ge melting (referred to as Thick Ge S/D Stressors earlier in Fig. 4), devices with MeltED or embedded Ge S/D exhibit a further 10% Iᵧᵧᵧᵧ enhancement (Fig. 11) as well as a further 15% peak Gᵧᵧᵧ improvement (Fig. 12). Since MeltED Ge S/D devices employ a slightly higher activation thermal budget, one might question if the enhancement is simply due to a decrease in effective channel lengths or S/D series resistances. Fig. 13 plots the cumulative distributions of SS, Rₓₓₓₓ and Gᵧᵧᵧᵧ for 2 sets of devices with similar mask gate lengths. It is quite clear that non-melted Ge and MeltED Ge devices have comparable short channel control and S/D series resistances (estimated from Rₓₓₓₓ at high gate overdrive), Iᵧᵧᵧᵧ characteristics in Fig. 14 show comparable SS and DBL between a MeltED Ge S/D and a Si S/D control device. Gᵧᵧᵧᵧ is clearly enhanced by ~22%. The MeltED Ge S/D device shows a dramatic 120% Iᵧᵧᵧᵧ enhancement over the Si S/D control device (Fig. 15). On average, the Iₓxx enhancement at an Iᵧᵧᵧᵧ of 1 x10¹⁷ A/m² obtained with the MeltED Ge technique is close to 100%.

Since the lattice mismatch between Ge and Si is 4%, the substrate compliance effects of narrow and thin SOI lines may not be able to completely suppress the formation of dislocations. It is important that such defects are formed outside the S/D depletion regions during transistor operation. Fig. 16 compares the junction leakage currents of Si Control, non-melted Ge S/D and MeltED Ge S/D devices. It is found that the leakage currents are quite comparable and are of a low magnitude. Energy dispersive spectrometry (EDS) of a MeltED Ge S/D nanowire’s S/D reveals uniform ~85% Ge concentration. It is postulated that as Ge melts, Si also dissolves in the molten Ge. In a SiGe core/shell nanowire S/D region, the small volume of Si can completely dissolve in the relatively much larger surrounding volume of molten Ge, leading to the formation of a uniform SiGe alloy upon re-crystallization. In this case, the seed for re-crystallization is located underneath the gate spacers. As a result, fully embedded Ge-rich SiGe stressors are formed in the S/D regions of nanowire devices. Iᵧᵧᵧᵧ transfer characteristics in Fig. 18 show comparable SS and DBL for MeltED Ge and non-melted Ge S/D nanowire devices. Such embedded stressors result in a further 16% Iᵧᵧᵧᵧ enhancement in the MeltED Ge S/D nanowire device, improving its drive current to 609 µA/m (Fig. 19). Note that such performance levels were achieved without S/D metatllization.

Conclusions

Pure Ge S/D stressors induce large compressive channel stress, enhancing hole mobility greatly. Substrate compliance effects result in larger Iᵧᵧᵧᵧ enhancement for narrow width nanowire devices compared to wider width devices. By employing a MeltED diffusion technique, dopant activation and stressor embedding was accomplished in a single process step, achieving Iᵧᵧᵧᵧ enhancement of ~100% and ~125% for planar UTB-FETs and nanowire-FETs respectively.

References

enhancement at a fixed small width to a control with raised Si S/D. UTB-FETs with are well-confined outside the extension regions. Impact junction leakage, indicating that defects transconductance was obtained at a DIBL of 75 mV.

Fig. 8. Ge S/D stressors result in 80% enhancement at a fixed DIBL of 1x10^7 A/µm. Ge stressors grown on S/D are unembedded. Raised Si S/D were used for all control devices.

Fig. 5. At DIBL of 1x10^7 A/µm, I_Dsat enhancement of 135% is larger than I_Dsat enhancement, as I_Dsat is less limited by series resistance.

Fig. 6. Mobility is very significantly enhanced by large compressive stress due to Ge S/D stressors. Peak transconductance is increased by 105% at a DIBL of 75 mV.

Fig. 9. New Melt-Enhanced Dopant (MeltED) diffusion and activation process. After shallow S/D implant and S/D capping, a 950°C spike anneal melts the Ge-rich region, and achieves these key objectives: Interface inter-diffusion embeds the Ge stressor; Dopant diffuses, redistributes uniformly, and is substitutionally incorporated as Ge recrystallizes.

Fig. 10. Sheet resistance measurements of MeltED Ge with 2 thicknesses. Both received surface BF2 implants only. Both films have near identical resistivity values, which confirm that Boron is uniformly diffused in the liquid Ge and is substitutionally incorporated as Ge recrystallizes.

Fig. 11. MeltED Ge S/D stressors are embedded, and gives a further 10% I_Dsat enhancement at DIBL of 1x10^7 A/µm, as compared to the unembedded Ge S/D stressors (also plotted in Fig. 4). Greater strain effects come with S/D stressor embedding.

Fig. 12. An additional 15% enhancement in peak transconductance was obtained at a DIBL of 75 mV as a result of increased channel strain.

Fig. 13. p-FETs with MeltED/Embedded Ge S/D have 22% higher C_Dsat than those with unembedded Ge S/D (not melted). All p-FETs have the same short channel control and L_D (35nm). R_D at high gate overdrive (V_G-S_D = 2.5V) estimates R_D to be comparable.

Fig. 14. I_Dsat-V_G plot showing comparable DIBL and SS for a p-FET with Raised Si Control and a p-FET with Embedded Ge S/D (MeltED).

Fig. 15. I_Dsat-V_G plot of same pair of devices in Fig. 14. Embedded Ge S/D (MeltED) gives a 120% I_Dsat enhancement over a p-FET with Si S/D.

Fig. 16. Ge S/D stressors do not significantly impact junction leakage, indicating that defects are well-confined outside the extension regions.