

## SERC Thematic Strategic Research Programme

---

### VLSI-PHOTONICS INTEGRATION TECHNOLOGIES & SYSTEMS WORKSHOP REPORT

---

#### 1. EXECUTIVE SUMMARY

<b>Title of Theme</b>	VLSI-Photonics Integration Technologies & Systems
<b>Date and Venue</b>	September 11-12, 2003 @ IMRE Auditorium
<b>No. of Participants</b>	94
<b>Local Convenor</b>	Prof Daniel Chan, NUS Prof Yoon Soon Fatt, NTU
<b>Panel Members</b>	Professor Ray Chen, University of Texas at Austin Professor Anthony Levi, University of Southern California Professor Elias Towe, Carnegie Mellon University

The workshop served as a platform for the local research community to hear from the experts and to share their research work, as well as for surfacing the local capabilities and gaps in this area.

Arising from the workshop, the expert panel felt that Singapore has good work at the components level and that the infrastructure is excellent. The timing now is right for systems-level work, where opportunities are ripe for Singapore to consolidate our capabilities in devices and processes to achieve world excellence in this area.

#### 2. WORKSHOP SCOPE

Silicon-based Very Large-Scale Integrated (VLSI) electronics are the foundation of modern microsystems technology. Rapidly increasing processing speeds and system complexity need to be accompanied by increases in data transmission rates between chips and between systems. Recent advances in the development of innovative integration solutions that involve VLSI and photonic systems offer much potential for increased performance. In parallel, the development and exploitation of new integration technologies that provide seamless intimate incorporation of photonic materials and devices with silicon, while maintaining compatibility with silicon fabrication process technology, is of great relevance.

Research in VLSI-photonics would typically include the development of new emitters, detectors, optical waveguides, integrated sensors, photonic A/D converters, smart pixel arrays in order to provide the useful solutions that involve optical interconnections in conjunction with photonic devices heterogeneously integrated on a VLSI platform. This will enable a semiconductor die to have overall capabilities that greatly exceed what would be achievable with currently available integration techniques.

Acknowledging that VLSI photonics is a potentially wide theme, the scope of the workshop was therefore focused on encompassing the following areas:

- **Architecture:** Circuit architectures for heterogeneously integrated photonic systems, such as multifunction ICs, novel architectures for I/O intensive and high connectivity bandwidth applications,
- **Integration Issues & Challenges:** Monolithic and heterogeneous integration techniques for optical interconnects, including free space interconnect solutions, integration with surface emitters, 2-D and 3-D chip-scale large integration of optical interconnections and their scalability issues which addresses device and process integration concerns,
- **Novel fabrication and processing techniques:** Microassembly of photonic devices on VLSI platforms addressing alignment and self-assembly processes, new functional materials, new epitaxial methods compatible with VLSI platforms.

### **3. HIGHLIGHTS OF THE PRESENTATIONS**

The workshop featured presentations from the local research community and the international expert panelists, thereby facilitating technical exchanges among the researchers and fostering possible collaborations among them. The presentations given by the local research community showcased some of their existing and future work in “VLSI-Photonics Integration Technologies and Systems”. The following are the highlights from these presentations, categorised under the two sub-themes – a) Integration Issues and Challenges and b) Novel Fabrication and Processing Techniques.

#### **A) INTEGRATION ISSUES AND CHALLENGES**

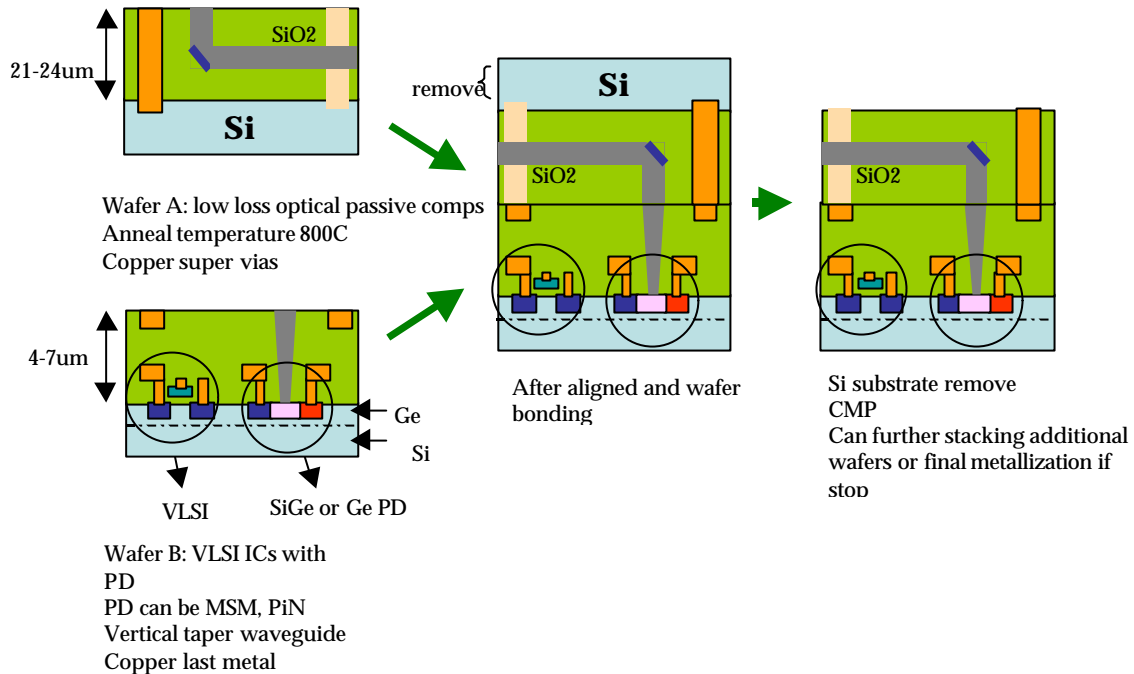
##### **Silicon based VLSI Photonics Technologies**

In future environment, people will have constant access to a variety of services, such as entertainment, personal communications, tele-education, etc...anywhere and anytime. The realization of such intelligence network structure that links people and services will require large capacity links, high transmission rate, efficient and very reliability network management, and low cost.

In optical components for *access network*, requirements for transmitters, fibers, regenerators, switches, and receivers in the next 5-10 years are *highly integrated components* at distribution nodes and *very low cost* plug-and-play Tx and Rx and optical network unit (ONU) that operate at 10Gbit/s and beyond. Silicon-based VLSI-photonics will be one of the key technologies to realise these requirements. Depending on the chosen wavelength for access networks - 850nm, 1.3um or 1.5um, hybrid integration or monolithic integration approaches maybe used. The Institute of Microelectronics (IME) is currently pursuing the research in these areas.

In the hybrid approach that combines III-V based photodetectors, laser diodes with silica-based optical passive components and Si-based optical transceivers (i.e. transimpedance amplifier (TIA), clock data recovery (CDR), and modulator driver),

3-D chip scale large integration schemes such as wafer to wafer bonding through copper “super via” may be deployed. This technology improves alignment accuracy through single step global alignment, reduces assembly and packaging processing steps, and reduces footprint. Higher performance and lower cost ONU can therefore be realized. This heterogeneous integration is illustrated in Fig.1.



**Fig.1 Proposed VLSI-Photonics Heterogeneous Integration**

courtesy of Mr Doan My The, Institute of Microelectronics

The monolithic approach may further reduce cost. In this approach, SiGe or Ge photodetectors are integrated with SiGe or Ge transistors and extremely high index silica (i.e. bending radius is 20 μm) optical passive components. To address the quantum efficiency and response speed of the photodetector and a laser diode for a complete photo-transceiver, modular researches in Ge based quantum dots PD & LD and nano-heteroepitaxial growth of InGaAs on buffer SiGe and Si substrate are other possible topics for researches.

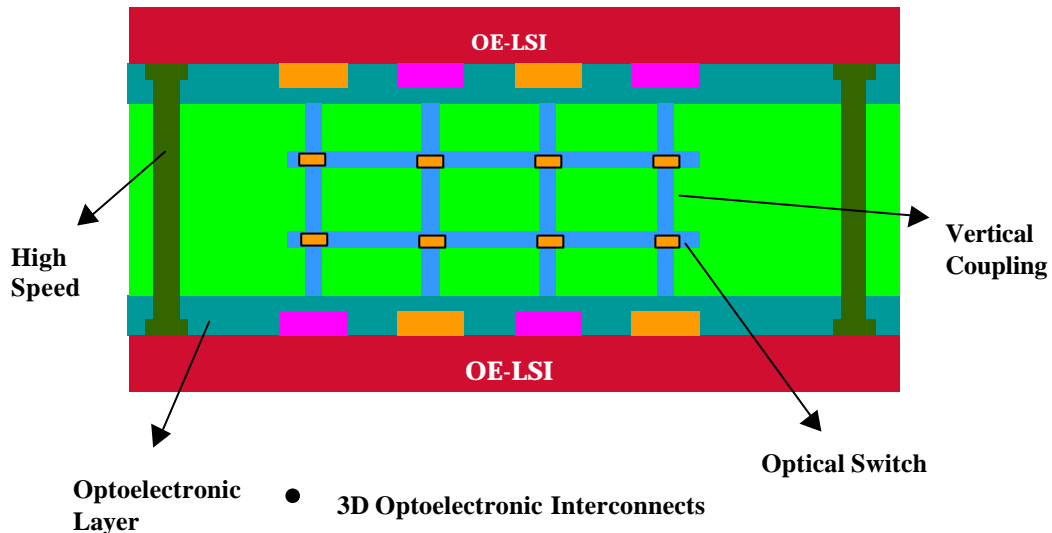
### **Three-Dimensional Waveguides for Heterogeneous Integration of Optoelectronic Array Modules**

In today's gigascale integration era, interconnects have become the primary barrier on performance and efficiency. The three-dimensional heterogeneous integration of Si electronics, optoelectronic devices and planar light wave circuits presents a promising solution to increase data bandwidth whilst achieving reduction in power dissipation and improved signal integrity.

#### ***Design and Simulation***

A new three-dimensional interconnection concept was proposed by Dr Albert Lu Chee Wai (Singapore Institute of Manufacturing Technology) for the realization of optoelectronic array modules (see Fig. 2). Conventional planar interconnects inhibit optical routability in large array modules, resulting in degraded signal integrity. By using vertical optical interconnects, this barrier can be alleviated. Finite-difference time-domain (FDTD) simulations will be carried out to extract the interconnections characteristics and to provide reconfigurable component libraries.

**Fig. 2 3D Stacked Optoelectronic Array Module**



Courtesy of Dr Albert Lu Chee Wai, Singapore Institute of Manufacturing Technology

**Waveguide Fabrication**

As a key enabling technology for three-dimensional interconnect realization, a novel approach of waveguide processing is proposed. The use of femtosecond laser pulses to directly induce refractive index changes in optical materials is gaining significant attention. By focusing the femtosecond laser beam inside the material and traversing either the beam or sample, lines with a change in refractive index can be induced within the focal volume of the beam. Due to the selective modification by the femtosecond laser pulses, index changes can be induced at any depths inside an optical material and essentially offers the ability to fabricate three-dimensional waveguides.

Using this technique, the Singapore Institute of Manufacturing Technology (SIMTech) has successfully fabricated waveguides and 1x4 splitters in fused silica and aluminosilicate glasses with transmission losses as low as 1 dB/cm at 1550 nm. By controlling the laser processing conditions, waveguides of controllable cross sectional dimensions (3-100 μm) and shapes (circular or elliptical) can be achieved.

In addition, SIMTech has developed a fabrication process for thick UV-patternable hybrid sol-gel films by using spin-coating method. Buried channel waveguides were realized with different coating composition and a large refractive index difference of

0.05 was obtained between the core and the cladding layer. Direct laser writing on the sol-gel coatings will be explored.

### ***Test Bed Development***

A parallel channel optical communication system will be developed. VCSEL based transceivers and fabricated waveguides to validate Gigabit duplex interface performance including the measurement of wavelength and polarization dependent characteristics. This test bed will also form a unique platform to characterize future chip-to-chip and board-to-board interconnection schemes.

## **B) NOVEL FABRICATION AND PROCESSING TECHNIQUES**

### **Integration of GaAs/Si with Ge or GOI buffer layer and its impact on device integration**

Even though silicon technology dominates the electronics industry, it has its limitations. Its ability to emit light is poor and significant innovations are necessary to compete with III-V compounds for light emitter applications. It also has a limited ability to deliver higher speeds that the new applications are beginning to demand, particularly with the increasing demand of data rate for Internet access. On the other hand, III-V compounds such as GaAs show promise due to their superior electrical and optical characteristics, power efficiency and high switching speed. However, the GaAs compound materials also have their shortcomings, such as small wafer size, weak mechanical strength, etc, which result in higher cost of their wafers and devices. Thus, a combination of the advantages of GaAs and Si would meet a demand and would open a new door for the semiconductor industry.

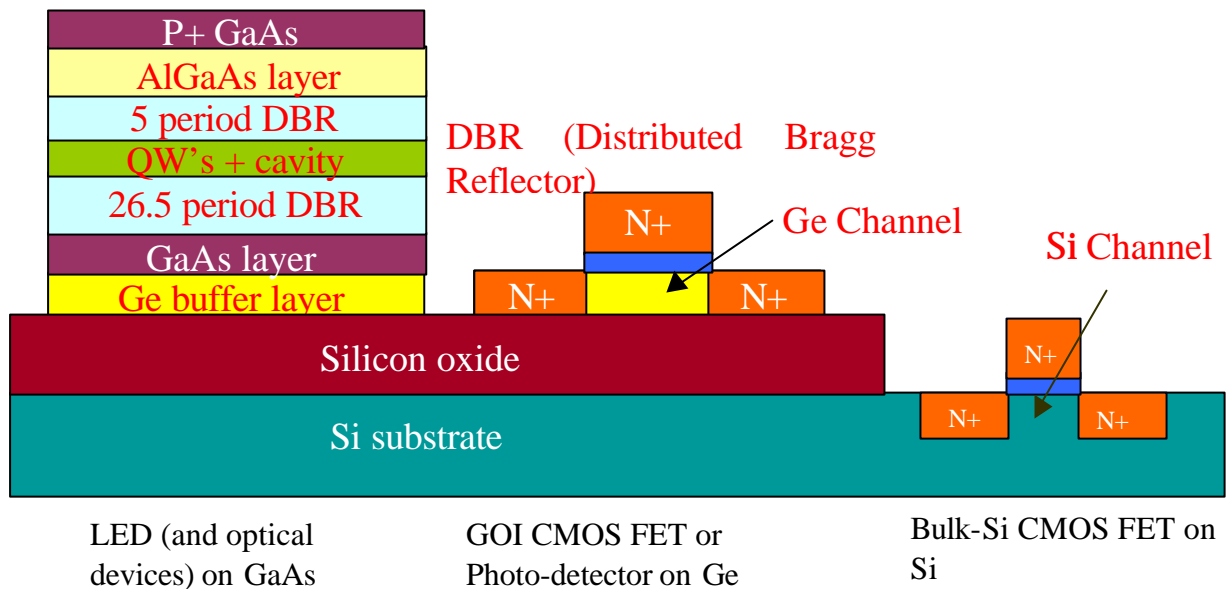
The pursuit of Si and GaAs integration, having begun in the early 1980s, has not been fully implemented at the commercial level, although some progress has been achieved. The difficulties are mainly thermal expansion and lattice constant differences between the two materials. Germanium was found to have a lattice constant (5.6575 Å) very close to that of GaAs (5.6533 Å), suggesting that it is a very promising material for integration with GaAs. The integration of GaAs on Ge substrate was demonstrated by a research group at University of Gent, Belgium. However, bulk-Ge MOSFETs have high leakage currents due to the narrow band-gap, which makes it difficult to integrate CMOS devices.

The research team<sup>1</sup> at Silicon Nano Device Laboratory (SNDL), National University of Singapore has demonstrated that a MOSFET with GOI (germanium-on-insulator) on Si substrate can reduce the leakage current significantly. The research team is exploring to develop integration technology of GaAs on Si substrate with Ge or the new developed GOI as a buffer layer. The challenge of this proposal will be the growth of GaAs on Ge, as GaAs has a polar structure while Ge is a non-polar structure and this can cause lattice mismatch problem when growing layers. With

---

<sup>1</sup> CX Zhu, Li MF, G Samudra, BJ Cho, WJ Yoo, SJ Lee, YC Yee, Albert Chin, and TP Dim-Lee Kwong

the development of GaAs/Ge (or GOI)/Si system, the team is able to combine the advantages of GaAs and Si on the same chip. The developed technology will make it possible to create a new class of wafers and devices that combine the best properties of silicon (robust and cost efficiency) with the best properties of compound semiconductors (optical capabilities and high speed). To demonstrate the whole concept, the team proposes to realize high speed photonic transceiver ICs on Si by integrating the light source, photonic detector, and transistors using the integration technology of GaAs/Ge (or GOI)/Si system on the same chip (see Fig. 3).



**Fig. 3 Integration of GaAs on Si with GOI Buffer Layer: A platform for Device Integration**

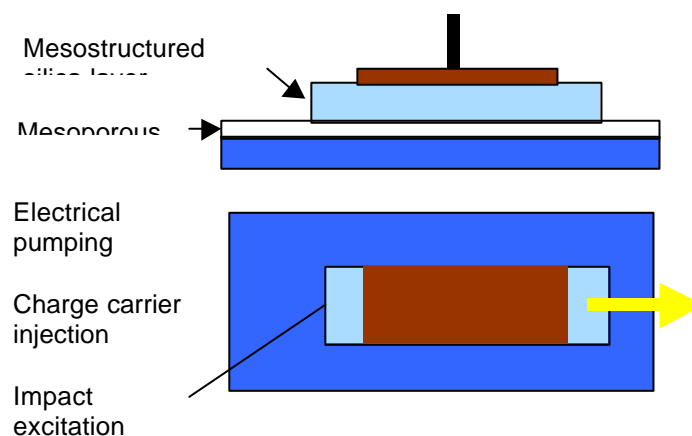
Courtesy of Dr Zhu Chunxiang, Silicon Nano Device Laboratory, National University of Singapore

### Mesoporous silica and silicon germanium heterostructures for optoelectronic applications

As an important challenge in VLSI-optoelectronic integration is the development of a light emitter based on silicon-related materials, the absence of such emitters has resulted in the present heterogeneous integration approach where compound semiconductor devices are bonded to the silicon IC after the last interconnect level has been completed. This hybrid process is more costly. For applications in the long term and for basic science, it would be desirable to have group IV emitters that can be integrated directly with silicon devices. There are two possible approaches. The first uses the modified band structure of nanostructured silicon to increase the likelihood of radiative interband transitions. The second circumvents the indirect bandgap nature of silicon altogether by using Si-SiGe superlattices in a quantum cascade structure. The emission characteristics is determined by the layer thickness and the material optical properties is not important.

A research team<sup>2</sup> at Nanyang Technological University (NTU), School of EEE has recently developed two techniques for fabricating porous silica and organosilicate dielectrics. These porous dielectrics are used as ultra low dielectric constant inter-metal dielectrics for deep submicron integrated circuits. The first method is based on a multistep sol-gel process and the second is based on a dendrimer templating technique. Both approaches involve solution synthesis consisting of spin-on processing and post-deposition curing and dehydroxylation. A dielectric constant of  $\sim 2$  has been obtained by both synthetic routes. Separately, the team has used chemical vapor deposition technique to grow strained SiGe and Si-SiGe heterostructures on silicon. These include single quantum wells and superlattices (up to 10 periods) on Si. Preliminary characterization results have been obtained.

The team is proposing to extend the research in the present work in two complementary directions. The first one involves using the pores in the dielectrics as receptacles for the embedding of optically active molecular species such as laser dyes or nanoparticles. The incorporation of the optically active species will involve chemical co-assembly during the templated synthesis. In a recent report, amplified spontaneous emission has been obtained by optical pumping. The team plans to further develop this processing route and investigate the possibility of electroluminescence from these hybrid materials (see Fig. 4). The work on SiGe heterostructures can be extended to include the design and epitaxial growth of a quantum cascade structure for holes. A main focus will be the growth of metamorphic (strain relaxed) SiGe for the subsequent fabrication of the multiple superlattice periods. For the quantum cascade device, emission wavelength can extend to far infrared or terahertz region. Since the operating frequencies of integrated circuits are steadily approaching this region, these sources may have applications for future interconnects.



**Fig. 4 Proposed Device for Electroluminescence Observation**  
 Courtesy of Wong Kin Shun Terence, Nanyang Technological University

<sup>2</sup> TKS Wong, BK Ng, K Pita, Q Ngo, AQ Liu

## ANNEX: Workshop Programme

11 September 2003

Time	ACTIVITY	
<b>9.00 am</b>	<b>Registration</b>	
9.30 am	Introduction to SERC VLSI-Photonics Integration Technologies & Systems workshop	Dr Lim Kiang Wee, Director, SERC
9.40 am	Opening remarks	Prof Daniel Chan (NUS)
9.50 am	Optical Interconnects in Future Systems	Prof Anthony Levi (USC)
10.30 am	Multichannel Gigabit photonic modules for Passive Optical Network and Datacom applications	Dr Mahadevan K Iyer (IME)
10.50 am	Three-dimensional waveguides for heterogeneous integration of optoelectronic array modules	Dr Albert Lu (SIMTech)
11.10 am	Integration of GaAs/Si with Ge or GOI buffer layer and its impact on device integration	Dr Zhu Chunxiang (NUS)
<b>11.30 am</b>	<b>Lunch cum poster viewing</b>	
1.30 pm	Nanostructures for advanced photonics	Prof Elias Towe (CMU)
2.10 pm	Mesoporous silica and silicon germanium heterostructures for optoelectronic applications	A/Prof Wong Kin Shun, Terence (NTU)
2.30 pm	Development of silicon nano-crystals thin films for silicon based lasers	Dr Yu Siu Fung (NTU)
<b>2.50 pm</b>	<b>Tea Break</b>	
3.20 pm	Optical interconnects within a box and future projection	Prof Ray Chen (UT at Austin)
4.00 pm	Silicon-based VLSI photonics technologies	Mr Doan My The (IME)
4.20 pm	Wrap up of day one	Prof. Yoon Soon Fatt (NTU)
4.30 pm	End of day one	