Process Design Kit (PDK) for 2.5D Through Silicon Interposer (TSI) Design Enablement &

2.5D TSI Cost Modeling

2.5D TSI Characterization and Modeling Team
Outline

- Technology to Design Enablement: The Ecosystem
- IPD Devices: Resistors, Capacitors and Inductors
- 2.5D TSI Technology Modeling and Characterization
- 2.5D TSI Design Enablement & Methodology
- Deliverables: PDK and 2.5D TSI Design Enablement
- 2.5D TSI Cost Modeling
- Deliverables: 2.5D TSI Cost Modeling
Technology to Design Enablement: The Ecosystem
Technology to Design Enablement:
Ecosystem for evolving Technologies such as 2.5D TSI

- RC models using simulations/analytical models
- RC measurements & characterization using technology vehicle
- Verified RC models confirming characterization results inside IME PDK
- Physical design EDA flow for 2.5D TSI design enablement
- Leveraging the design flow for design optimization

Constant interaction between Technology, Characterization and Design groups to develop trustworthy IME PDK & EDA flow
IME’s 2.5D TSI Consortium on August 17, 2012

PDK Elements:
- Technology/Viewer Files (.tf/.drf)
- Library Components/Integrated Passive Devices (IPDs)
  - Resistor
  - Capacitor (MIMCAP)
  - Spiral Inductor
- TSI Component RC Models:
  - Micro-bumps
  - M1-M4 BEOL
  - TSV
  - RDL Layer
  - C4 bump
- DRC/LVS/PEX Rule decks

Scope of Work: Integrate the PDK components streamlining 2.5D TSI design process
IPD Devices: Resistors, Capacitors and Inductors
Integrated Resistors

- IME’s thin film resistor process

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<tr>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Ti</td>
<td>43</td>
<td>8.6</td>
<td>300mm</td>
<td>250</td>
<td>2</td>
<td>17.2</td>
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</tbody>
</table>

- Deposition Temperature: 180°C

Applications:
- DC Biasing
- Termination

Scope of Work: Design and Parameterized Cell implementation
Characterization across layout variations
### Integrated Capacitors

#### IME’s Metal-Insulator-Metal Capacitor (MIM)

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<tbody>
<tr>
<td>Si₃N₄</td>
<td>7.5</td>
<td>300mm</td>
<td>300-500</td>
<td>2.21-1.32</td>
<td>2 -12µm</td>
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</table>

**Applications:**
- DC isolation
- AC bypass
- Power Distribution Network
- Filtering,
- Impedance matching

**Scope of work:** Design and Parameterized Cell implementation
Characterization across layout variations
# Integrated Spiral Inductors

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Meander</th>
<th>Loop</th>
<th>Spiral</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductance</td>
<td>Medium</td>
<td>Low</td>
<td>High</td>
</tr>
</tbody>
</table>

- **Favorable due to wide inductance range**

### Integrated Inductor Prototype
- **Tape out in year 2012**

### Table

<table>
<thead>
<tr>
<th>W [µm]</th>
<th>S [µm]</th>
<th>L [nH]</th>
<th>Q&lt;sub&gt;max&lt;/sub&gt;</th>
<th>SRF [GHz]</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>2</td>
<td>7.5</td>
<td>9.8</td>
<td>2.59</td>
</tr>
<tr>
<td>16</td>
<td>16</td>
<td>4.8</td>
<td>8.5</td>
<td>3.23</td>
</tr>
</tbody>
</table>

- **Defined by technology:**
  - \( W_{\text{min}} - W_{\text{max}} = 2-16\mu m; S_{\text{min}} - S_{\text{max}} = 2-16\mu m \)
  - Stack-up aligned with electrical design:
    - Metal thickness: 2µm; Dielectric (SiO₂) thickness: 2µm
    - Area: Dimension 0.5 x 0.5mm²; 5.5 turns

### Scope of work:
- Design and Parameterized Cell implementation
- RF Characterization across layout variations
2.5D TSI Technology Modeling and Characterization
## RC Estimations using Analytical Models

<table>
<thead>
<tr>
<th>Parasitic RC Elements:</th>
<th>Resistance</th>
<th>Capacitance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Micro bump</td>
<td>2.4mΩ</td>
<td>0.7fF</td>
</tr>
<tr>
<td>M1/M2/M3/M4 (interline)</td>
<td>4.2Ω/mm</td>
<td>34fF/mm</td>
</tr>
<tr>
<td>M1/M2/M3/M4 (line-to-ground)</td>
<td>4.2Ω/mm</td>
<td>34/13.8/7.6/5.31fF/mm</td>
</tr>
<tr>
<td>TSV (C_{ox}) / TSV (C_{TSV})</td>
<td>21.4mΩ</td>
<td>120fF/80fF*</td>
</tr>
<tr>
<td>RDL (interline)</td>
<td>280mΩ/mm</td>
<td>15.9fF/mm</td>
</tr>
<tr>
<td>RDL (line-to-ground)</td>
<td>280mΩ/mm</td>
<td>34fF/mm</td>
</tr>
<tr>
<td>C4 Bump (line-to-ground)</td>
<td>2.4mΩ</td>
<td>116.84fF</td>
</tr>
</tbody>
</table>

### Analytical RC estimations for 2.5D TSI Design to be implemented in PDK Rev0.0 → To be verified using TSI characterization suite

**Assumptions:**
- Minimum Size wires considered
- Ground substrate for TSV & C4 bump capacitance assumed
- *Electrical Characterization & Modeling of Through Silicon Via (TSV) for 3D ICs; G. Katti et al.; TED; Jan. 2010
Impact of isolation thickness on C4 bump capacitance

Increased Isolation Thickness → Reduced C4 bump capacitance
Initial isolation specification 1µm increased to 2µm to reduce C4 Bump capacitance from ~120fF → 60fF
**Component RC characterization using C-V and I-V measurements to verify/update the RC models**

**Resistance Measurements:**
- Four point resistance measurements using I-V meter

**Capacitance Measurements:**
- C-V and C-t measurements using LCR meter

**RF Measurements:**
- Network Analyzer

**Scope of Work:** To design a comprehensive test structure characterization suite for model verification and PDK implementation
2.5D TSI Design Enablement Methodologies

2.5D TSI Physical Design Flow
- Auto PnR
- Timing Verification
- Power Ground Network Analysis
- Sign-off .gds

Package & PCB Design Flow
- Package Design
- SI and PI verification
- System sign-off

Electrical Domain

Thermo Mechanical simulations
- Warpage Estimation
- Thermal Fatigue Analysis

Mechanical/Thermal Domain

Thermal simulations
- Thermal Map/Hot spot Estimation
- Heat Sink Design
- Thermal System sign-off

Scope of Work: Leveraging established EDA tools for 2.5D TSI Design
Evaluate 3D IC EDA tools for 2.5D platform

Potential Tools
- Synopsys
  - ICC
  - Astro
- Cadence
  - Virtuoso
  - SOC Encounter
  - SiP
- Mentor Graphics
  - Calibre
Physical Design (EDA) Flow for 2.5D TSI Design

Objective: To Develop EDA Flow enabling external partners to design novel 2.5D TSI chips leveraging 2.5D TSI technology.

- **Synthesized Netlist**
  - Floor planning & Placement of µBumps and C4 bumps (in sync with guest die & package specs) [Co-Design]

- **Timing/Power Verification**
  - Design Constraints Specifications
  - DRC/LVS rule decks

- **DRC/LVS Verification**
  - DRC/LVS rule decks

- **Sign off Flow(.gds)**

- **Routing on 2.5D TSI**
  - Component RC Models in PEX rule decks

- **Parasitic Extraction**

**Features:**
- Auto placement and routing of TSVs
- TSV is considered as a device for PEX
- Clock Tree Synthesis (CTS)
- Platform for design exploration and optimization
IC, Package & PCB Co-design Flow

1. Identifying package/PCB (BGA/Direct Attach)
2. Import TSI Connectivity
3. Auto Spider Route
4. SI & PI Verification (Time & Frequency Domain Analysis)
5. Package/PCB Design sign-off

*Not a true representation
FPGA & Memory integration on TSI – A Case Study

- **FPGA & Memory Auto placement**
- **Auto-routed Design with TSVs**
- **Schematic/Netlist Entry**
- **Package to IC timing verification**
- **Eye Diagram Verification on TSI**
Deliverables: PDK & 2.5D TSI Design Enablement

- PDK with Rev0.0 RC models, IPDs & DRC/LVS/PEX implementation
- Design and tape out 2.5D TSI technology characterization vehicle
- Verification of electrical models with test vehicle characterization → Models implementation within PDK Rev 1.0
- Corner analysis employing min-typ-max RC values
- Develop a design flow to enable external partners to leverage 2.5D TSI technology
  - IC, Package and PCB co-design
  - Auto placement and routing of TSVs
  - Routability/congestion analysis
  - SI/PI Analysis
  - Platform to optimize 2.5D TSI Designs
2.5D TSI Cost Modeling
“Cost” is the most important factor to mainstream 2.5D TSI technology

- Materials
- Process flow
- Equipments
- RDL, UBM & C4 Bump technologies
- Labor cost
- Line Infrastructure
- # Metal Layers
- TSV Architecture
- Die Area

Manufacturing cost needs to be estimated
2.5D TSI Cost Modeling

TSV Formation

- Via Etch
- Via Isolation
- Via Fill

Base Model: Yole
To be calibrated & enhanced within consortium

BEOL Processing

- Single Damascene
- Dual Damascene

Base Model: Yole
To be calibrated within consortium

TSV Reveal

- Temporary Bonding
- Thinning

Base Model: Yole
To be calibrated & enhanced within consortium

Bump & RDL Formation

- UBM
- RDL
- C4 bump processing

Base Model: Yole
To be calibrated within consortium

TSV Formation & TSV Reveal → TSV cost model
BEOL processing → BEOL cost model
RDL processing → RDL cost model
UBM, C4 Bump processing → Bump cost model

2.5D TSI Cost = Cost of { TSV Formation & Reveal + BEOL processing + UBM, RDL & C4 bump formation}
Cost of TSV formation & reveal varying with Manufacturing Volume and Yield

Volume and Yield are critical to reduce cost

Assumptions:
Location: Singapore
Processing line: 300mm
TSV Architecture: 12x100µm

Source: Yole
Cost of TSV formation & reveal

**Assumptions:**
- Location: Singapore
- Processing Line: 300mm
- Volume: 500k wafers/year (HVM)
  - 10k wafers/year (LVM)
- Yield: 85%

**Wafer Cost ($)**

*Wafer Cost varying with TSV Architectures*

**Observations:**
- Huge variation (~5.25x) with volume between LVM and HVM
- TSV filling is the most expensive process
- TSV Reveal cost is independent of TSV Height

**Example:**
12x100µm TSV formation and reveal wafer cost demonstrates huge variation with volume: $1075 (LVM) → $205 (HVM)

Source: Yole

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IME’s TSI Consortium on August 17, 2012
Cost Estimations:
- 2.5D TSI wafer (4 BEOL layers and 1 RDL) manufacturing cost = $470 (HVM) & $2470 (LVM)
- Estimated 2.5D TSI FPGA & Memory Interposer (25x30mm) die cost = $6 (HVM) & $35 (LVM)

Estimated cost per wafer (Assumptions):
- BEOL processing = $35 per metal layer (HVM)
- RDL processing = $35 (HVM)
- UBM and C4 bump processing = $90 (HVM)

LVM Cost = 5.25x HVM Cost

Scope of Work: 2.5D TSI Cost Model Calibration
Deliverables: 2.5D TSI Cost Modeling

- TSV formation and TSV reveal cost to be calibrated/enhanced
  - Invariant cost variation with wafer thickness → to be confirmed (to be enhanced if required)
  - Support PECVD

- Work with consortium members to incorporate BEOL and RDL, UBM and C4 Bump cost
  - Is RDL significantly cheaper than BEOL?

- Cost comparison of two 2.5D TSI systems
Thank you

Q & A