Institute of Microelectronics
A*STAR

11 Science Park Road, Singapore Science Park II, Singapore 117685

Si Wafer Fab Services

200mm CMOS Fab (1000 sq.m Class-100)

200mm MEMS Fab (450 sq.m Class-100)

300mm TSV Fab (1200 sq.m Class-10)

Assembly/Packaging (375 sq.m Class- 100 & 10K)

- **Un-Patterned Si Wafers (200mm/300mm)**
- **Patterned Si Wafers (200mm/300mm)**
- **Chemicals/Photo Chemicals Evaluation**
- **Semiconductor Materials Evaluation**
- **Assembly/Packaging Services**
- **Si Wafer back-grinding services (200mm/300mm)**
- **Customized Solutions**

200mm CMOS Fab:
200mm CMOS Fab is a Silicon-Based wafer processing Integrated Facility equipped with 248nm KrF DUV high throughput Lithography tool, Ion Implanter, epitaxial tool, and Metallization Tools for barrier/gate/silicide, Electroplating Tools, Rapid Thermal Annealing, PECVD Tools, CMP Tools, ALD and integrated in-line metrology tool set.

200mm MEMS Fab:
Our MEMS FAB is equipped with advanced 200mm Si Micro-fabrication facility with MEMS specific process technologies. MEMS Fab is a 200mm Silicon-Based wafer processing Integrated Facility consisting of MEMS Tools such as ASML Stepper, Double-sided aligner, Metal PVD Moly/AlN Cluster Tool, Plasma Cluster DRIE(Si/Di-electric/Metal/PRS), Bonder cluster tool and integrated in-line metrology tool set.

300mm TSV IME-AMAT Joint Lab:
IME has set-up "Center of Excellence in Advanced Packaging" Jointly with Applied Materials, USA. The 12" Fab line is equipped with 300mm Silicon-Based TSV Process Modules, such as Bridged Stepper, Coater Track, ECP Tool Set, Annealing, Curing Furnaces, Clean-tech, PVD Charger UBM. We are setting-up TBDB Cluster tool for both 200mm & 300mm wafer bonding/de-bonding with in-situ pre-bond clean capability.

Advanced Lithography Technology Development:
Offers services for 200mm Si wafer Advanced Lithography Processing in state-of-the-art Class-10 Wafer Fab in IME. We offer ArF Photo Resists Coating (Coater Track from Tokyo Electron Limited, Japan) & ArF Resist Fine Lithography Patterning of 100nm features (193nm Nikon Scanner S-306). Supported by in-line CD & overlay measurement capabilities.

Packaging Assembly:
Lab is equipped with advanced packaging tools to support various packaging technologies such as wire bonding, flip chip, fan-out WLP, Chip-to-wafer, chip-to-chip , chip to substrate bonding and chip stacking using micro bump bonding. We can offer the following service support for small volume samples build for proto typing and testing.

- **Lithography**
  -248/193nm
  -Stepper
  -Aligner
- **Furnaces**
  -Thermal Oxide
  -LPSiN&TEOs
  -Poly Silicon
  -Wet Oxidation
- **CVD**
  -USG
  -HDP Oxide
  -Silicon-Nitride
  -PE-TEOS/PSG
  -Amorphous-Si
- **PVD**
  -Copper Seed
  -Ta/TaN
  -Al,AlO2
  -Ti/TiN
  -HfO2/HfN
- **ECPs**
  -RDL (Ni/Sn/Au)
  -TSV Cu/Pillar
  -Cu Damascene
- **CMP**
  -Dielectrics
  -Poly-Si
  -Polyimide
  -Copper CMP
- **Packaging**
  -Wafer Thinning
  -Sawing (dicing)
  -Die-attach
  -Wire-bonding
  -Flip chip bonding
  -Underfilling
  -Gold stud bumping
  -Dage X-ray Inspection
- **Bonding**
  -PB-TB
  -De-Bond

For All Enquiries Please Contact fabservices@ime.a-star.edu.sg :: IME website: www.ime.a-star.edu.sg