Packaging Platforms and Solutions

As device scaling powered by Moore’s law faces challenges in meeting industry requirements, advanced packaging and interconnect technologies have emerged as an alternative solution to achieve performance, power, form-factor, and cost requirements that are critical to key industry drivers such as mobile, 5G, data centres, automotive, and IoT.

IME offers a wide range of advanced packaging technology solutions to address the above industry needs. Our platforms include 2.5D through-silicon interposer, 3D TSV, fan-out wafer level packaging, MEMS wafer level chip-scale packaging, fine-pitch Cu pillar, chip-on-wafer (direct Cu-to-Cu) bonding, electronic-photonic integration, as well as thermal solutions.
Wafer Level Packaging for Mobile, 5G, and Internet-of-Things (IoT)

Advanced electronic packages need to address the growing interconnect gap between IC and PCB. Achieve a high level of functional integration, and meet form-factor, power, cost, and electrical performance requirements. Fan-out wafer level packaging with fine pitch multi-level RDL and through-mold interconnects enables multi-chip integration, package-on-package (PoP), integrated passives including RLC/antenna and ultra-thin profile to meet the above requirements.

IME has established a full-fledged 300mm FOWLP development line to develop novel packaging structures and process integration flows for next generation applications including mobile-AP, 5G mmWave antenna-in-package, multiple MEMS/sensors for IoT, ASIC+HBM heterogeneous integration, and automotive electronics. IME has also developed MEMS wafer level chip-scale packaging (WLCSP) platform which enables low-cost integration of capped MEMS device and CMOS ASIC device without TSVs. This packaging platform can be used for timing devices, inertial sensors, and RF MEMS packaging.

IME is also working with the industry ecosystem to develop fan-out panel level packaging (FOPLP) technology based on mold-first and RDL-first approaches to provide high-throughput and cost-effective manufacturing solution through panel processing.
High performance applications such as data centres, high performance computing, 3D image sensors, advanced memories, and artificial intelligence cube require 2.5D/3D integration based on TSV and interposer technology to meet performance and power requirements.

IME has established 2.5D/3D TSV/through-silicon interposer (TSI) platform technology consisting of critical building blocks including PDK, 3D-TSV fabrication flow, thin wafer handling, as well as assembly and packaging. This has led to the successful development of end-to-end solutions for 2.5D heterogeneous integration of logic and memory, chip-on-wafer bonding for image sensors, and wafer-to-wafer bonding for high density memories. In addition, IME has developed cost-effective 2.5D/3D IC solutions through our low-cost interposer platform, active TSI, and TSV-free interposer platforms for heterogeneous integration.

**Capabilities**
- Large area through-silicon interposer (TSI) for heterogeneous integration
- Active interposer and TSV-free interposer for low-cost 2.5D system integration
- Wafer level micro bumping up to 20µm pitch using Cu pillar with SnAg
- CoW using Cu-Cu bonding (up to 6µm pitch)
- 3D chip stacking (up to 15 chips of 15x15mm²)
- Via-last TSV for image sensor and logic-logic stacking
- Wafer-to-wafer hybrid bonding
- Wafer level memory stacking

**Image Descriptions**
- Cross-sectional view of 2.5D Si interposer with 3-layer RDL on front side, 10x100µm TSV and 8GA on backside.
- 6µm pitch TSV Cu pillars directly bonded to Cu RDL.
- Demonstrated 15 chip stacking using 20µm pitch micro bump interconnections.
Increasing bandwidth requirement is driving the need for 400G optical interconnects in modern data centres, which in turn drives integration of electronic ICs and photonic ICs to achieve smaller form-factor with improved signal integrity and higher data rate. Optical transceiver (TRx) module using EPIC packaging can be applied for on-board optics (OBD), quad small form-factor pluggable (QSFP) double density, and octal small form-factor pluggable (OSFP) with data rate 400G and beyond for optical links within and in-between data centres. Application of TSVs with flip-chip bonding electrical interconnection in EPIC packages can greatly improve signal integrity with smaller form-factor compared to conventional approaches.

IME has demonstrated key capabilities such as <0.5μm misalignment tolerance laser diode (LD) integration on silicon photonic IC, thermal management for QSFP packaging, and RF optimization 56Gbps/ch. IME is currently developing a compact and robust electronic-photonic integrated circuit (EPIC) packaging solution based on 2.5D interposers and 3D TSV for 400G applications.

**Capabilities**

- Laser diode integration on PIC (coupling loss <2.7dB)
- High-speed RF management (3dB bandwidth >50GHz)
- Thermal management solution for quad small form-factor pluggable (QSFP) (3.5W) and octal small form-factor pluggable (OSFP) (10W)
- EPIC packaging with 2.5D interposer and 3D TSV
- 56Gbps Si-photonics passive and active device integration
- Design, fabrication, and test of high-speed TSV and RDL in SOI wafer
Thermal Management and Cooling Solutions for product-oriented applications

Thermal management is critical to modern electronic packages. In smartphones, data centres, and power electronics, a key challenge is to provide optimized product-oriented cooling solutions that can meet form-factor and thermal performance requirements. To meet these requirements, thermal management needs to be handled at the chip level and at the board/system level. At the chip level, IME has demonstrated active-liquid cooling technology for >350W/cm². At the system level, smart liquid cooling can achieve cooling solutions of up to 21kW per rack for data centre application. In addition, IME is exploring the application of advanced thermal interface materials (TIM) such as 3D-graphene, for heat removal from 3D stacks achieved through TSV and PoP.

- Thermal modeling/simulation to design chip level and system level cooling solutions
- Passive cooling strategy featuring high density 3D-graphene TIM for TSV/PoP stacks
- Active cooling technology featuring Si-based hybrid micro-cooler to achieve >350W/cm² for high performance ICs and smart liquid cooling to achieve >21kW/rack
- Thermal characterization to JEDEC standards
Services and Infrastructure

- Advanced packaging turnkey solutions for industry applications
- Thermo-mechanical, electrical, and thermal modeling and simulations to provide design guidelines
- TSV and through-silicon interposer (TSI) fabrication for 2.5D/3D IC packaging
- TSV fabrication and assembly for image sensor applications
- MEMS wafer level chip-scale packaging
- FOWLP demonstration for new products
- FOWLP re-constructed wafers for equipment and material evaluations

Infrastructure

- 3000m² of cleanrooms
- 200mm and 300mm TSV engineering line
- 300mm FOWLP development line
- Assembly and packaging lab
- Package/board level reliability testing and failure analysis facilities

One-Stop Solution from System Concept, Design Integration, Fabrication & Testing to Final Packaging

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IME’s Multi-Chip FOWLP Development Line

IME’s full fledged development line comprises state-of-the-art tools including PVD chamber for seed layer deposition, PR track for photoresist coating and photo-dielectric coating, stepper for lithography, developer track, plating (Cu, Ni, Au, SnAg), wet bench for PR stripping, spray etcher for seed etching, N2 furnace for curing, O2 plasma for descum/etch, flip-chip bonder for chip-to-wafer bonding, molding tool for wafer level compression, warpage adjuster for molding tape de-bonding and warpage adjustment, backgrinder for wafer thinning, laser de-bonder for carrier de-bonding, solder jetter for solder ball attach, and wafer dicer for wafer sawing.

IME is committed to protect customer’s IP and confidentiality

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