Institute of Microelectronics
A*STAR

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A*STAR'S IME CONSORTIUM DEVELOPS INNOVATIVE ADVANCED PACKAGING SOLUTIONS FOR HIGHER PERFORMANCE AND EFFICIENCY IN CONSUMER AND HIGH POWER ELECTRONICS

IME and industry partners overcome limitations of IC packaging to enable higher density packages for more powerful and efficient electronic systems

Singapore — Following the launch of the 12th Electronics Packaging Research Consortium (EPRC12) in 2013, A*STAR's Institute of Microelectronics (IME) and 11 of its consortium partners across the semiconductor supply chain have developed novel solutions in integrated circuit (IC) packaging. (For the list of consortium members, please refer to **Annex A**).

The consortium has achieved its objectives of developing novel solutions to overcome the reliability and performance issues and technical challenges in packaging solutions for compact sized consumer electronics and high power electronics. To achieve this, the consortium leveraged IME's capabilities in wafer level packaging, assembly processes and thermo-mechanical modelling as well as the constant feedback from the industry players.

These solutions allow for high density packaging that enables greater system capabilities, such as increased memory and bandwidth and faster processing speed, paving the way for more powerful and efficient systems in consumer devices and high power electronics.

Improving reliability in packaging which utilises Cu/low-k interconnects

The consortium successfully reduced the high thermo-mechanical stress that is generated in the assembly of IC packaging that adopts Cu pillars and low-k chips.

This was demonstrated through thermal compression bonding for large size chip (18x18mm chip) and package (25mm x 25mm FCBGA package).

The consortium reduced the pitch size of Cu pillars on a two-layer low cost organic substrate and bare Cu bond pads from 40µm to 30µm through thermal compression bonding. This process not only enables higher density interconnects but also enables the bonding of Cu pillar to bare Cu bond pads without traditional NiAu plating or organic solder preservative coating on Cu bond pads, leading to lower substrate costs.

A modeling methodology and a set of design guidelines were devised to help manufacturers create low-stress generating package designs. With these innovative advanced packaging solutions, packaging which utilises Cu/low-k interconnects becomes a viable option for further system scaling in the next generation computing and portable electronics such as smart phones and tablets.

Enabling smaller form factor in 3D Fan-out Package-on-Package (3D PoP)

The consortium reduced the existing package profile of the 3D Fan-out Package-on-Package to achieve higher power efficiency and cost-effectiveness across a wide range of consumer mobile applications including mobile devices, tablets, laptops and digital cameras.

This was achieved by removing the substrate on the Printed Circuit Board (PCB) that carries the passive components supporting electrical performance, and embedding these components within the package. The innovative technique which employs a Redistribution Layer (RDL) process flow and a Through Mold Via technology, reduces the package profile by approximately 25 per cent to achieve a higher density package, and also reduces the manufacturing cost by approximately 15 per cent.

Improving thermal management and power efficiency in high power electronic systems

The consortium has devised innovative packaging technologies to improve thermal management and power efficiency of high power electronic systems.

By applying a zinc-based high temperature soldering process and material optimisation, the consortium has managed to raise the maximum junction

temperature of the TO-220, which is commonly used for high power switching device packaging, from 170°C to 245°C.

Thermal management capabilities were also demonstrated in a double-sided cooling power inverter module. The consortium utilised a flip-chip bonding and compression molding process to create a flat structure which serves as a thermally conductive path for both top and bottom surfaces of a power inverter module. This innovative process enables thermal resistance of up to 0.18 W/K, surpassing the conventional single-sided cooling modules by approximately 40 per cent.

The consortium achieved a 30 per cent height reduction in lead frame based Intelligent Power Modules (IPMs), enabling higher integration of power devices, control IC and passive components within a more compact package. This was achieved through a cost-effective technique of replacing the lead frame found in the IPMs with a thin and fine layer substrate and metal layer structure.

“These technology breakthroughs signify the consortium’s potential to keep pace with the rapid trends of advanced packaging. Through close collaboration with our industry partners, we have overcome technical hurdles to achieve smaller form factor and higher performance for next generation applications. IME will continue to contribute its research capabilities to develop timely solutions,” said Prof. Dim-Lee Kwong, Executive Director of IME.

“Heraeus have been working with IME through the different EPRC consortia for the past few years in developing new solutions to keep up with the emerging trends in the industry. The EPRC12 has helped Heraeus in understanding the challenges and requirements of high temperatures die attach materials and the processes, allowing us to address the industry's unmet needs in high temperature Pb free die attach materials for power device packaging”, said Dr. Zhang Xi, Head of Global R&D Bonding Wire, HET- Innovation, Heraeus Materials, Singapore Pte Ltd.

“Fan-Out Wafer Level Packaging (FOWLP) is a key technology for the semiconductor industry. By achieving the process development of dual side RDL on mold wafer and polymer filling on TMV (Through Mold Via) for FO PoP, the consortium helped us to understand the process requirement and overcome the material development challenges”, said Mr Takayoshi Suzuki, General Manager, Tokyo Ohka Kogyo, Singapore.

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About A*STAR's Institute of Microelectronics (IME)

The Institute of Microelectronics (IME) is a research institute of the Science and Engineering Research Council of the Agency for Science, Technology and Research (A*STAR). Positioned to bridge the R&D between academia and industry, A*STAR IME's mission is to add value to Singapore's semiconductor industry by developing strategic competencies, innovative technologies and intellectual property; enabling enterprises to be technologically competitive; and cultivating a technology talent pool to inject new knowledge to the industry. Its key research areas are in integrated circuits design, advanced packaging, bioelectronics and medical devices, MEMS, nanoelectronics, and photonics.

For more information on IME, please visit www.ime.a-star.edu.sg.

About the Agency for Science, Technology and Research (A*STAR)

The Agency for Science, Technology and Research (A*STAR) is Singapore's lead public sector agency that spearheads economic oriented research to advance scientific discovery and develop innovative technology. Through open innovation, we collaborate with our partners in both the public and private sectors to benefit society.

As a Science and Technology Organisation, A*STAR bridges the gap between academia and industry. Our research creates economic growth and jobs for Singapore, and enhances lives by contributing to societal benefits such as improving outcomes in healthcare, urban living, and sustainability.

We play a key role in nurturing and developing a diversity of talent and leaders in our Agency and Research Institutes, the wider research community and industry.

A*STAR oversees 18 biomedical sciences and physical sciences and engineering research entities primarily located in Biopolis and Fusionopolis.

For more information on A*STAR, please visit www.a-star.edu.sg.

Annex A

Members of the 12th EPRC Consortium:

The 12th EPRC Consortium was launched in 2013 and includes the following and two other packaging companies:

- Ajinomoto
- EV Group
- GLOBALFOUNDRIES
- Heraeus Materials
- Henkel
- Infineon Technologies
- JSR Micro N.V.
- Linxens,
- Tokyo Ohka Kogyo