Frequency-Thermal Characterization of On-Chip Transformers With Patterned Ground Shields

Jinglin Shi, Wen-Yan Yin, Senior Member, IEEE, Kai Kang, Jun-Fa Mao, Senior Member, IEEE, and Le-Wei Li, Fellow, IEEE

Abstract—Extensive studies on the performance of on-chip CMOS transformers with and without patterned ground shields (PGSs) at different temperatures are carried out in this paper. These transformers are fabricated using 0.18-μm RF CMOS processes and are designed to have either interleaved or center-tapped interleaved geometries, respectively, but with the same inner dimensions, metal track widths, track spacings, and silicon substrate. Based on the two-port S-parameters measured at different temperatures, all performance parameters of these transformers, such as frequency- and temperature-dependent maximum available gain ($G_{\text{max}}$), minimum noise figure ($NF_{\text{min}}$), quality factor ($Q_1$) of the primary or secondary coil, and power loss ($R_{\text{loss}}$) are characterized and compared. It is found that: 1) the values of $G_{\text{max}}$ and $Q_1$ factor usually decrease with the temperature; however, there may be reverse temperature effects on both $G_{\text{max}}$ and $Q_1$ factor beyond certain frequency; 2) with the same geometric parameters, interleaved transformers exhibit better low-frequency performance than center-tapped interleaved transformers, whereas the center-tapped configurations possess lower values of $NF_{\text{min}}$ at higher frequencies; and 3) with temperature rising, the degradation in performance of the interleaved transformers can be effectively compensated by the implementation of a PGS, while for center-tapped geometry, the shielding effectiveness of PGS on the performance improvement is ineffective.

Index Terms—Interleaved and center-tapped transformers, maximum available gain, minimum noise figure, pattern ground shields (PGSs), power loss, quality ($Q$) factor, temperature.

I. INTRODUCTION

Silicon monolithic transformers have been widely used in designs of on-chip impedance matching, balun, low-noise amplifier feedback, and other microwave and millimeter-wave components, e.g., such as those introduced in [1]–[4]. Based on different layouts, several types of on-chip silicon transformers and their modeling and optimization were studied over the past few years [5]–[11]. Simburger et al. proposed two analytical transformer models for both tapped and stacked geometries [2], and Niknejad and Meyer presented a lumped-element equivalent-circuit model for interleaved planar transformers [5]. More recently, some significant progresses in the development of novel CMOS transformers have been achieved, and among these, the optimized design of a distributed active transformer [12], 30–100-GHz transformers fabricated using SiGe BiCMOS technology for millimeter-wave integrated circuits [13], and a new compact model for monolithic transformers in silicon-based RF integrated circuits (RFICs) [14] are good examples. Similar to silicon-based spiral inductors, silicon-based transformers also suffer from serious power losses at high frequency. The loss mechanisms can be summarized into five categories, which are: 1) skin effects; 2) proximity effects; 3) eddy-currents in the substrate; 4) shunt conduction current flowing in the substrate; and 5) lateral conduction currents flowing in the substrate between the primary and secondary coils. The first three mechanisms are due to time-varying magnetic fields, whereas the remaining two are caused by time-varying electric fields. The losses due to time-varying magnetic fields can be efficiently reduced by increasing the electric conductivity of metals and using a slightly doped substrate with higher resistivity or implementing patterned magnetic shields.

In order to reduce losses in the silicon substrate due to the time-varying electric field at a high frequency, one practical way is to employ an appropriate patterned ground shield (PGS), which provides a short terminal to the electric field leaking into the substrate. In some previous studies [15]–[18], it was demonstrated that metal grid shields can be used to effectively reduce mode attenuation of microstrip or coplanar interconnects. For silicon-based spiral inductors, Yue and Wong first presented a PGS spiral inductor model in 1998 [19]. In 2002, Yim et al. further examined the effects of a PGS on the performance of spiral inductors [20]. In particular, novel patterned trench isolation with a floating p/n junction and floating metal poles were also implemented underneath reference spiral inductors [21]. For spiral inductor cases, although the implementation of the PGS may increase the parasitic capacitance, it makes the design more independent of substrate dopant concentrations and can reduce noise coupling into substrate. Therefore, an appropriate choice of the embedding depth of the PGS is very important in the effective implementation of the PGS. However, accurately characterizing frequency- and temperature-dependent PGS transformers has not yet been well conducted. In the design of a transformer, there are multiple choices in its configuration, such as interleaved, center-tapped interleaved, and even stacked...
geometries. The performance parameters of a transformer, such as maximum available gain \(G_{\text{max}}\), self-resonance frequency, minimum noise figure \(\text{NF}_{\text{min}}\), and power losses \(P_{\text{loss}}\) are all sensitive to the variation of temperature, parameters, i.e., \(\omega\), of the primary and secondary coils. For comparison, the \(\omega\) parameters measured at temperatures, the values of \(G_{\text{max}}, \text{NF}_{\text{min}}, P_{\text{loss}},\) and the \(Q_1\) factor are extracted and compared. Some conclusions are finally drawn in Section V.

II. ON-CHIP PGS TRANSFORMERS

Fig. 1(a) and (b) shows the top view of an interleaved PGS transformer and a center-tapped interleaved PGS transformer fabricated on a silicon substrate using 0.18-\(\mu\)m RF CMOS processes with the same internal dimension of \(D = 60 \mu\)m, metal track width of \(W = 10 \mu\)m, track spacing of \(S = 1.5 \mu\)m, and the same PGS implemented as shown in Fig. 1(c) (where the width and spacing of the PGS metal bar are \(W_p = S_p = 0.4 \mu\)m). The turn numbers of the primary and secondary coils are designed to be \(N = 3\) and \(4\), respectively. For comparison, a group of non-PGS (NPGS) transformers with the same geometric parameters \(\{D, W, S, N\}\) as its counterpart was also designed, fabricated, and examined.

III. MODIFIED TEMPERATURE-DEPENDENT EQUIVALENT-CIRCUIT MODELS

For an interleaved transformer with or without a PGS, its temperature-dependent small-signal equivalent-circuit model can be obtained based on the circuit model given in [22], as shown in Fig. 2. In Fig. 2(a) and (c), the capacitances \(C_{\text{ox1}}\) and \(C_{\text{ox2}}\) can be well treated as temperature-independent elements, due to the constitutive characteristics of silicon oxide, whereas the series self-resistances \(R_{m1,m2}(T)\) of the primary and secondary coils, the silicon substrate resistances \(R_{b1,b2}(T)\), and shunt capacitances \(C_{b1,b2}(T)\) are all sensitive to the variation of temperature. For example, \(C_{b1}(T)\) and \(C_{b2}(T)\) decrease with temperature, while \(R_{b1}(T)\) and \(R_{b2}(T)\) increase with temperature.

At a low frequency, the series equivalent self-inductances \(L_{m1}(T)\) and \(L_{m2}(T)\) and series resistances \(R_{m1}(T)\) and \(R_{m2}(T)\) in Fig. 2(a) can be calculated based on the Z-parameters converted from the \(S\)-parameters, i.e.,

\[
\begin{align*}
R_{m1}(T) & = \text{Re}[Z_{11}(T)] \\
R_{m2}(T) & = \text{Re}[Z_{22}(T)] \\
L_{m1}(T) & = \frac{\text{Im}[Z_{11}(T)]}{\omega} \\
L_{m2}(T) & = \frac{\text{Im}[Z_{22}(T)]}{\omega}.
\end{align*}
\]

The coupling coefficient is defined as \(k(T) = k_r(T) + jk_m(T)\), and the mutual resistive \(k_r\) and reactive \(k_m\) coupling factors are calculated by [8]

\[
\begin{align*}
k_r(T) & = \frac{|\text{Re}[Z_{12}(T)]|^2}{|\text{Re}[Z_{11}(T)]| \cdot |\text{Re}[Z_{22}(T)]|} \\
k_m(T) & = \frac{|\text{Im}[Z_{12}(T)]|^2}{|\text{Im}[Z_{11}(T)]| \cdot |\text{Im}[Z_{22}(T)]|}.
\end{align*}
\]
where $\text{Re}(\cdot)$ and $\text{Im}(\cdot)$ represent real and imaginary parts of the $Z$-parameters, respectively. As pointed out in [8], the mutual resistive factor $k_m$ mainly accounts for the hybrid effects of parasitic capacitances and eddy currents in the silicon substrate. The $Q$ factor for primary and secondary coils can be evaluated by

$$Q_{1,2}(T) = \frac{\text{Im}[Z_{1,22}(T)]}{\text{Re}[Z_{1,22}(T)]}$$  \hspace{1cm} (4)$$

while the self-resonance frequency of the transformer is defined at which $Z_{11}$ or $Z_{22}$ of the device first becomes purely resistive. It is especially known that one of the important performance indicators of a transformer is its maximum available gain, which is defined by [22]

$$G_{\max}(T) = \left| \frac{S_{21}(T)}{S_{12}(T)} \right| \frac{n - \sqrt{n^2 - 1}}{2}$$  \hspace{1cm} (5)$$

where

$$n = \frac{1 - |S_{11}(T)|^2 - |S_{22}(T)|^2 + |\Delta|^2}{2 |S_{12}(T)S_{21}(T)|}$$  \hspace{1cm} (6a)$$

and

$$\Delta = S_{11}(T)S_{22}(T) - S_{12}(T)S_{21}(T)$$  \hspace{1cm} (6b)$$

or [21]

$$G_{\max} = 1 + 2(\sqrt{x^2 + x^2})$$  \hspace{1cm} (7a)$$

and

$$x = \frac{\text{Re}(Z_{11}(T)) \cdot \text{Re}(Z_{22}(T)) - [\text{Re}(Z_{12}(T))]^2}{[\text{Re}(Z_{12}(T))]^2 + [\text{Im}(Z_{12}(T))]^2}.$$  \hspace{1cm} (7b)$$

The minimum noise figure $NF_{\min}$ of a transformer is defined by [22]

$$NF_{\min} = 10\log(1/G_{\max}),$$  \hspace{1cm} (8)$$

The circuit model of an interleaved NPGS transformer (Design 1) is plotted in Fig. 2(a). At high frequencies, it can be further simplified as the form shown in Fig. 2(b), where $R_{e1,2}(T)$, $L_{e1,2}(T)$, $R_{M}(T)$, and $L_{M}(T)$ represent the equivalent primary and secondary resistances and inductances, and mutual resistances and inductances between them, respectively (where $i = 1$ and 2), and

$$R_{e1}(T) = \frac{\frac{R_{m1}(T)}{[\omega L_{m1}(T)]^2 + R_{m1}(T)} + 1}{R_{st1b}}$$  \hspace{1cm} (9a)$$

$$L_{e1}(T) = \frac{R_{m1}^2(T) + \omega L_{m1}(T)}{\omega^2 L_{m1}(T)}$$  \hspace{1cm} (9b)$$

$$C_{1}(T) = C_{si1}(T) + C_{o1} \frac{1 + \omega^2 [C_{o1} + C_{h1}(T)] C_{h1} R_{e1}(T)}{1 + \omega^2 (C_{o1}^2 + C_{h1})^2 R_{e1}^2(T)}$$  \hspace{1cm} (9c)$$

$$R_{st1b} = \frac{1}{\omega^2 R_{st1b}[C_{o1}^2 + C_{h1}]^2}$$  \hspace{1cm} (9d)$$

From Fig. 2, it can be found that the $Q$ factors of primary and secondary coils can be determined by

$$Q_i = \frac{\omega L_{e1}(T)}{R_{e1}(T)}$$  \hspace{1cm} (9e)$$

or [21]

$$G_{\max} = \frac{G_{\max}}{\frac{R_{st1b}(T)}{R_{m1}(T)}} \frac{R_{st1b}(T)}{R_{st1b}(T) + [\omega L_{m1}(T)/R_{m1}(T)]^2 + 1} \frac{R_{m1}(T)}{R_{st1b}(T) + [\omega L_{m1}(T)/R_{m1}(T)]^2 + 1}$$  \hspace{1cm} (9f)$$

Equation (9g) indicates that the substrate loss factor will approach unity as $R_{st1b}(T)$ increases infinitely. In other words, an infinite value of $R_{st1b}(T)$ may result in a high $Q$ factor of the primary or secondary coil, and $R_{st1b}(T)$ is determined by (9f). As $R_{st1b}(T)$ goes to zero or infinitely, $R_{st1b}(T)$ will become infinite. This means that making the substrate either short or open can enhance the $Q$ factor. In this paper, our methodology is to short the substrate by inserting a PGS between the transformer and substrate so as to block electrical fields from penetrating into the silicon substrate.
For an interleaved PGS transformer (Design 1), its circuit model is plotted in Fig. 3. In Fig. 3, there are two paths to the ground, i.e., through the PGS and silicon substrate, respectively. We can change the interconnects of $C_{ox1}(C_{ox2})$, $C_{b1}(C_{b2})$, and $R_{b1}(R_{b2})$ into a shunt branch of a capacitance and resistance. Similarly, we can also change $C_{FGS1}(C_{FGS2})$ and $R_{FGS1}(R_{FGS2})$ into a similar shunt branch. Thus, a simplified circuit model will be obtained, which can be easily compared to that in the NPGS case. The element $C_{re1}(C_{re2})$ in Fig. 3 is derived from the $C_{FGS1}(C_{FGS2})$, $C_{ox1}(C_{ox2})$, $C_{b1}(C_{b2})$, $R_{b1}(R_{b2})$, and $R_{FGS1}(R_{FGS2})$. $R_{m1}(R_{m2})$ and $C_{b1}(C_{b2})$ are not only from the silicon substrate; they also include the effects of $R_{FGS}$ and $C_{FGS}$. Hence, the temperature coefficients of these elements for a PGS transformer will not completely follow the characteristics of the silicon substrate.

For an NPGS transformer of Design 2, its lumped-element equivalent-circuit model is shown in Fig. 4. The elements $R_{m1}(R_{m2}(T))$ and $L_{m1}(T)(L_{m2}(T))$ represent the series resistance and inductance of the primary (secondary) coil, respectively; three capacitances $C_{12}$, $C_{13}$, and $C_{21}$ are utilized to describe the capacitive coupling effect between primary and secondary coils; $R_{m3}(T)$ and $L_{m3}(T)$ are the series resistance and inductance of the center-tapped metal track; $C_{ox1}(C_{ox2})$, $C_{b1}(C_{b2})$ and $R_{b1}(R_{b2})$ have the same meanings as indicated above. Following a similar procedure as shown in Fig. 3, the circuit model for a PGS transformer of Design 2 can also be obtained, but suppressed here. The center $T$ portion represents the low-frequency model, while the remaining part represents the high-frequency model.

At low frequencies, the elements in Fig. 4 satisfy a set of equations as follows:

$$\begin{align*}
R_{m1}(T) + j\omega [L_{m1}(T) + M(T)] &= Z_{11} - Z_{12} \\
R_{m2}(T) + j\omega [L_{m2}(T) + M(T)] &= Z_{22} - Z_{12} \\
R_{m3}(T) + j\omega L_{m3}(T) &= Z_{12}.
\end{align*}$$

Therefore,

$$\begin{align*}
R_{m1}(T) &= \text{Re}[Z_{11} - Z_{12}] \\
R_{m2}(T) &= \text{Re}[Z_{22} - Z_{12}] \\
R_{m3}(T) &= \text{Re}[Z_{12}] \\
L_{m3}(T) &= \text{Im}[Z_{12}]/\omega.
\end{align*}$$

Since the inductance and resistance depend on both physical and geometric parameters of the structure, and due to the symmetry between the primary and secondary windings, we can assume that

$$\frac{L_{m1}(T)}{L_{m2}(T)} = \beta \frac{R_{m1}(T)}{R_{m2}(T)}$$

where the parameter $\beta$ is given in [23] and its value can be determined using the curve-fitting technique based on the measured data. We then obtain

$$\begin{align*}
L_{m1}(T) &= \frac{\beta \text{Re}[Z_{11} - Z_{12}]}{\beta \text{Re}[Z_{11} - Z_{12}] - \text{Re}[Z_{22} - Z_{12}]} \frac{\text{Im}[Z_{11} - Z_{12}]}{\omega} \\
L_{m2}(T) &= \frac{\beta \text{Re}[Z_{22} - Z_{12}]}{\beta \text{Re}[Z_{11} - Z_{12}] - \text{Re}[Z_{22} - Z_{12}]} \frac{\text{Im}[Z_{11} - Z_{12}]}{\omega} \\
M(T) &= \frac{\text{Im}[Z_{11} - Z_{12}]}{\omega} - L_{m1}(T).
\end{align*}$$

At high frequencies, the two-port $Y$-parameters of the model in Fig. 4 can be obtained from the extrinsic $Z$-parameters, and

$$Z_{ex} = Z_m - Z_s$$

where $Z_m$ represents the $Z$-parameter obtained experimentally, and $Z_s$ is derived using (10a)–(10c).

The coupling capacitance $C_{12}$ between Port 1 and Port 2 can then be calculated by

$$C_{12} = \text{Im}[Y_{ex12}]/\omega.$$
and $a_2 = 3 \times 10^{-5}$ (298 K $\leq T \leq$ 500 K). Based on (18), we can easily evaluate the total temperature-dependent series resistances of the primary and secondary metal coils by

$$ R_{m,i}(T) = R_{\text{underpass}}(T) + R_{\text{coil},i}(T) $$  \hspace{1cm} (19a) 

where

$$ R_{\text{underpass}}(T) \approx \frac{L_{\text{underpass}}}{\frac{1}{2}\sigma(T)W}\left(1 - e^{-\mu_i/\delta(T)}\right) $$  \hspace{1cm} (19b) 

$$ R_{\text{coil},i}(T) \approx \frac{L_{\text{coil},i}}{\frac{1}{2}\sigma(T)W}\left(1 - e^{-\mu_i/\delta(T)}\right) $$  \hspace{1cm} (19c) 

$$ \delta(T) = \frac{1}{\pi\sigma(T)\rho_i} $$  \hspace{1cm} (19d) 

while $L_{\text{underpass}}$ and $L_{\text{coil},i}$ ($i = 1$ and 2) are the underpass lengths at metal layer M5 and the primary and secondary coils at metal layer M6, respectively. Fig. 5 shows the calculated $R_{m,i}$ of the primary and secondary coils of transformers of Designs 1 and 2 at temperatures of $T = 298$ K, 333 K and 373 K, respectively.

It is shown that the rising effect of temperature on $R_{m,i}(T)$ is easily observable, which will further increase the power loss of metal coils. When the same inner empty dimension, metal track width, track spacing, and turn number are assumed, the total metal track length of the primary or secondary coils in Design 1 is slightly shorter than that in Design 2. Correspondingly, at a given frequency and a known temperature, the former series resistance of the primary coil is slightly smaller than that in Design 2. Obviously, $R_{m,i}$ increases with temperature, and it can be described by a linear equation as follows:

$$ R_{mp,ms}(T) = R_{mp,ms}(T_0)\left[1 + C_{mp,ms} \cdot (T - T_0)\right] $$  \hspace{1cm} (20) 

where $C_{mp}$ and $C_{ms}$ are two temperature coefficients of the primary and second coils, respectively, and are determined by

$$ C_{mp,ms} = \left[\frac{R_{mp,ms}(T_0)}{R_{mp,ms}(T_0) - 1}\right]. $$  \hspace{1cm} (21) 

From Fig. 5, it can be evaluated that $C_{mp,ms} \approx 0.0031$ K at $f = 1$ GHz, while $C_{mp,ms} \approx 0.0022$ K at $f = 10$ GHz. If the above transformers are made of copper, $C_{mp,ms} \approx 0.0029$ K at $f = 1$ GHz, while $C_{mp,ms} \approx 0.0020$ K at $f = 10$ GHz. Hence, $C_{mp,ms}$ is also frequency dependent; such a property has usually been neglected in most of the literature.

Fig. 6 shows the extracted series inductances $I_{mp}$ (333 K) and $I_{mp2}$ (333 K) of Design 1 with $N = 4$ using (2a) and (2b), where the simulated result is also plotted for comparative purposes.

<table>
<thead>
<tr>
<th>Metals</th>
<th>$a_0$</th>
<th>$a_1$</th>
<th>$a_2$</th>
<th>$a_3$</th>
<th>$a_4$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminum</td>
<td>19.69998</td>
<td>-0.10727</td>
<td>0.00025</td>
<td>-2.5913 x 10^{-7}</td>
<td>1.0016 x 10^{-10}</td>
</tr>
<tr>
<td>Copper</td>
<td>29.1115</td>
<td>-0.15643</td>
<td>0.00037</td>
<td>-3.9347 x 10^{-7}</td>
<td>1.5644 x 10^{-10}</td>
</tr>
<tr>
<td>Gold</td>
<td>18.08394</td>
<td>-0.0872</td>
<td>0.00019</td>
<td>-1.9114 x 10^{-7}</td>
<td>7.2377 x 10^{-11}</td>
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<td>Nickel</td>
<td>9.40567</td>
<td>-0.05317</td>
<td>0.00011</td>
<td>-1.2483 x 10^{-7}</td>
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<td>Silver</td>
<td>26.56717</td>
<td>-0.13164</td>
<td>0.00029</td>
<td>-2.9549 x 10^{-7}</td>
<td>1.1257 x 10^{-10}</td>
</tr>
<tr>
<td>Tungsten</td>
<td>9.59998</td>
<td>-0.05123</td>
<td>0.00012</td>
<td>-1.2046 x 10^{-7}</td>
<td>4.6332 x 10^{-11}</td>
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TABLE II
SiLICON RESISTIVITY VALUES AT DIFFERENT TEMPERATURES

<table>
<thead>
<tr>
<th>Temp(K)</th>
<th>250K</th>
<th>300K</th>
<th>350K</th>
<th>400K</th>
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<tbody>
<tr>
<td>( \rho_{Si} = 1 \Omega \cdot \text{cm} )</td>
<td>0.645643</td>
<td>0.936659</td>
<td>1.27445</td>
<td>1.653792</td>
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<tr>
<td>( \rho_{Si} = 10 \Omega \cdot \text{cm} )</td>
<td>7.034618</td>
<td>10.20539</td>
<td>13.8858</td>
<td>18.01893</td>
</tr>
<tr>
<td>( \rho_{Si} = 100 \Omega \cdot \text{cm} )</td>
<td>70.8751</td>
<td>102.8212</td>
<td>139.902</td>
<td>181.5441</td>
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</table>

TABLE III
EXTRACTED CIRCUIT PARAMETERS OF TRANSFORMER OF DESIGN 1 WITH \( N = 4 \)

<table>
<thead>
<tr>
<th>Temp(K)</th>
<th>( R_m(\Omega) )</th>
<th>( L_m(\mu H) )</th>
<th>( C_{12}(F) )</th>
<th>( C_{23}(F) )</th>
<th>( C_{ox1}(F) )</th>
<th>( C_{ox2}(F) )</th>
<th>( R_{bg}(\Omega) )</th>
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</thead>
<tbody>
<tr>
<td>253</td>
<td>5.3</td>
<td>2.63</td>
<td>6.0</td>
<td>140</td>
<td>110</td>
<td>120</td>
<td>280</td>
</tr>
<tr>
<td>298</td>
<td>6.0</td>
<td>2.63</td>
<td>6.0</td>
<td>140</td>
<td>110</td>
<td>90</td>
<td>350</td>
</tr>
<tr>
<td>333</td>
<td>6.7</td>
<td>2.63</td>
<td>6.0</td>
<td>140</td>
<td>110</td>
<td>70</td>
<td>470</td>
</tr>
<tr>
<td>373</td>
<td>7.3</td>
<td>2.63</td>
<td>6.0</td>
<td>140</td>
<td>110</td>
<td>52</td>
<td>630</td>
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<td>7.9</td>
<td>2.63</td>
<td>6.0</td>
<td>140</td>
<td>110</td>
<td>35</td>
<td>860</td>
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P  S

<table>
<thead>
<tr>
<th>Temp(K)</th>
<th>( R_m(\Omega) )</th>
<th>( L_m(\mu H) )</th>
<th>( C_{12}(F) )</th>
<th>( C_{23}(F) )</th>
<th>( C_{ox1}(F) )</th>
<th>( C_{ox2}(F) )</th>
<th>( R_{bg}(\Omega) )</th>
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<tr>
<td>253</td>
<td>5.2</td>
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<td>7.0</td>
<td>155</td>
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<td>7.0</td>
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<td>140</td>
<td>180</td>
<td>600</td>
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<td>333</td>
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<td>2.63</td>
<td>7.0</td>
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<td>140</td>
<td>170</td>
<td>650</td>
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<tr>
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<td>7.0</td>
<td>155</td>
<td>140</td>
<td>160</td>
<td>680</td>
</tr>
<tr>
<td>423</td>
<td>8.0</td>
<td>2.63</td>
<td>7.0</td>
<td>155</td>
<td>142</td>
<td>147</td>
<td>720</td>
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TABLE IV
EXTRACTED EQUIVALENT-CIRCUIT PARAMETERS OF TRANSFORMER OF DESIGN 2 WITH \( N = 4 \)

<table>
<thead>
<tr>
<th>Temp(K)</th>
<th>( R_m(\Omega) )</th>
<th>( L_m(\mu H) )</th>
<th>( C_{12}(F) )</th>
<th>( C_{23}(F) )</th>
<th>( C_{ox1}(F) )</th>
<th>( C_{ox2}(F) )</th>
<th>( R_{bg}(\Omega) )</th>
<th>( R_{m3}(\Omega) )</th>
<th>( L_{m3}(\mu H) )</th>
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<tbody>
<tr>
<td>253</td>
<td>5.5</td>
<td>2.7</td>
<td>85</td>
<td>110</td>
<td>130</td>
<td>130</td>
<td>130</td>
<td>0.54</td>
<td>0.12</td>
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<tr>
<td>298</td>
<td>6.1</td>
<td>2.7</td>
<td>85</td>
<td>110</td>
<td>95</td>
<td>180</td>
<td>180</td>
<td>0.60</td>
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<td>6.8</td>
<td>2.7</td>
<td>85</td>
<td>110</td>
<td>74</td>
<td>230</td>
<td>230</td>
<td>0.67</td>
<td>0.12</td>
</tr>
<tr>
<td>373</td>
<td>7.5</td>
<td>2.7</td>
<td>85</td>
<td>110</td>
<td>55</td>
<td>300</td>
<td>300</td>
<td>0.76</td>
<td>0.12</td>
</tr>
<tr>
<td>423</td>
<td>8.1</td>
<td>2.7</td>
<td>85</td>
<td>110</td>
<td>40</td>
<td>400</td>
<td>400</td>
<td>0.82</td>
<td>0.13</td>
</tr>
</tbody>
</table>

Similar to (20), \( R_{bg}(T) \) (where \( i = 1 \) and 2) can also be approximately described by

\[
R_{bg}(T) = R_{bg}(T_0) \left[ 1 + C_{osi} \cdot (T - T_0) \right]
\]

where \( C_{osi} \) is the temperature coefficient of the substrate resistance of silicon, and it was experimentally demonstrated in [25] that the sheet resistance per square of the silicon substrate increases linearly with temperature from a room temperature to as high as 250°C. Based on Arora’s model, the temperature-dependent densities of carrier and mobility in the silicon substrate can be described by [26]

\[
p = N_d = n_i \exp \left( \frac{q \phi_f}{kT} \right)
\]

\[
\varphi_f = \left( \frac{T}{T_0} \right) \varphi_f(T_0)
\]

\[
- \frac{kT}{q} \left[ 1.5 \ln \left( \frac{T}{T_0} \right) + \frac{1}{2k} \left( \frac{E_g(T_0)}{T_0} - \frac{E_g(T)}{T} \right) \right]
\]

\[
E_g(T) = 1.206 - 2.73 \times 10^{-4} T
\]

\[
\mu_0(300) = \mu_{\text{min}} + \frac{\mu_{\text{max}} - \mu_{\text{min}}}{1 + (N_d/N_0)^{2/3}}
\]

\[
\mu_f(T) = \mu_f(300K) \cdot \left( \frac{T}{300} \right)^{-3/2}
\]

where \( k \) is the Boltzmann constant, \( q \) is the unit electron charge in Coulomb, \( N_d \) is the total dopant concentration in silicon, the parameters \( \mu_{\text{max}}, \mu_{\text{min}}, \mu_{\text{dd}}, N_0 \), and \( \alpha \) have different values for different types of impurities [26], and the resistivity \( \rho_{Si} = (1/\sigma_{Si}) \) of silicon is given by

\[
\rho_{Si} = \frac{1}{qN_d T_0}.
\]

The coefficient \( C_{osi} \) in (22) is obtained by

\[
C_{osi} = \frac{1}{R_{bg}} \frac{dR_{bg}}{dT}.
\]

Therefore, the temperature-dependent resistivity of silicon is calculated and summarized in Table II, which is very sensitive to the change of temperature.

Tables III and IV also further summarize the extracted equivalent-circuit parameters shown in Figs. 2 and 3 for a transformer with \( N = 4 \) at different temperatures. The following observations can be made.

With respect to the NPGS transformer of Design 1, the implementation of a PGS will result in an increase of \( R_{bg1} \) and \( R_{bg2} \) by a factor of 1.4–2.5, and \( C'_{ox1} \) and \( C'_{ox2} \) will changed slightly. Thus, the increase of \( R_{bg1} \) and \( R_{bg2} \) can be useful for the enhancement of \( Q \) factors of the primary and secondary coils.

The reactive coupling factor \( \kappa_{mg}(T) \) is not sensitive to the variation of temperature, and it is approximately 0.75 for the transformers of Design 1 with or without PGS. It is found that
Due to the negligible effect of the PGS at low frequency. However, as frequency further increases, the values of both $Z_{11}$ and $Z_{12}$ of the PGS transformer increases much faster than those of the NPGS case due to the strong capacitive effect that resulted from the PGS. The frequency corresponding to the peak value of $Z_{11}$ ($Z_{12}$) moves from approximately 10 GHz for the NPGS transformer to 8 GHz for the PGS case.

Fig. 8 shows the extracted mutual resistive and reactive coupling factors $\kappa_r$ and $\kappa_m$ for the transformer (Design 1) of $N = 4$ at room temperature and 373 K. It is noted that $\kappa_m$ does not change significantly at low frequencies because it mainly accounts for the effect of magnetic coupling. On the other hand, the resistive coupling factor $\kappa_r$ is much more sensitive to the variation of frequency than that of $\kappa_m$. Over the frequency range below 6 GHz, the value of $\kappa_r$ of a PGS transformer is smaller than that of its NPGS counterpart.

IV. EXTRACTION OF PERFORMANCE PARAMETERS AND DISCUSSION

To globally capture the electromagnetic-thermal characteristics of the above transformers, i.e., Designs 1 and 2, four sets of samples are designed to have $W = 10 \mu m$, $D = 60 \mu m$, and $S = 1.5 \mu m$, fabricated on a 10-Ω · cm silicon substrate using 0.18-μm RF CMOS processes, including: 1) NPGS interleaved transformers; 2) NPGS center-tapped transformers; 3) interleaved transformers with a PGS at M1; and 4) center-tapped transformers with a PGS at M1. The frequency- and temperature-dependent on-wafer two-port $S$-parameters are, respectively, measured using an HP-8510C network analyzer, and Cascade Microtech ground–signal–ground (G–S–G) probes with a temperature-controlled chuck. The chuck temperature can be increased from 223 K to as high as 473 K. In order to reduce the effect of increasing temperature on the probe station during measurements for different temperatures, two-time calibrations at room and higher temperatures are done, respectively. For the NPGS transformer, the open pad structure has been used for deembedding, while for PGS transformers, the open pad together with the PGS was deembedded. The maximum available temperature-dependent on-wafer two-port $S$-parameters are calculated using a simple deembedding technique.
gain, minimum noise figure, power loss, and Q factor of the primary or secondary coil of transformers are further extracted and subsequently compared.

A. Maximum Available Gain ($G_{\text{max}}$)

Fig. 9(a) and (b) shows the $G_{\text{max}}$ of the interleaved transformers versus frequency at temperatures $T = 253, 298, 333,$ and $373$ K, respectively. In Fig. 9(a) and (b), the temperature is increased from $253$ to $298, 333,$ and $373$ K gradually, and the following is shown.

1) As frequency increases, the value of $G_{\text{max}}$ does not change monotonously, and at certain frequency represented by $f_{sr}$, $G_{\text{max}}$ reaches its minimum.

2) Over the frequency range of $0.5$ MHz to approximately $8.4$ GHz in Fig. 9(a), $G_{\text{max}}$ decreases with temperature. However, as frequency increases higher than $8.4$ GHz, there is significant temperature reverse effect and $G_{\text{max}}$ increases with temperature.

3) Although the implementation of a PGS at the M1 metal layer has little effect on the maxima of $G_{\text{max}}$ ($N = 4$), the curves of $G_{\text{max}}$ in the PGS case at different temperatures become much flatter, as shown in Fig. 9(b). The decrease of $G_{\text{max}}$ is mainly contributed by the increase of the conductive loss due to imperfect metal coils. Since the silicon conductivity decreases with temperature, the substrate loss will be reduced at a higher temperature, which has a positive effect on $G_{\text{max}}$.

A comparison of the implementation of the PGS on $G_{\text{max}}$ is further demonstrated in Fig. 10(a) and (b) for a transformer (Design 2) with $N = 4$. In Fig. 10(a), a similar reverse temperature effect is observed, as shown in Fig. 9(a). As the frequency exceeds $f_{rs} \approx 16.4$ GHz, $G_{\text{max}}$ increases with temperature. On the other hand, it should be noted that the reverse frequency ($f_{rs}$) for Design 2 is much higher than that of Design 1.

Since the transformers of Designs 1 and 2 are designed to have the same geometrical parameters, i.e., $D = 60$ $\mu$m, $W = 10$ $\mu$m, and $S = 1.5$ $\mu$m, it is worthwhile to find out the difference in terms of $G_{\text{max}}$ versus frequency. Fig. 10 shows that the $G_{\text{max}}$ of Designs 1 and 2 with $N = 3$ at $T = 253$ and
333 K, respectively. As seen in Fig. 10, when the operating frequency is lower than the cross-point frequency $f_{ct} \approx 5.25$ GHz at $T = 253$ K, the $G_{\text{max}}$ of Design 1 is larger than that of Design 2. When the operating frequency further increases, however, a reverse effect is observed and the $G_{\text{max}}$ of Design 2 becomes larger than that of Design 1. When $T = 333$ K, $f_{ct} \approx 5.65$ GHz. Hence, it can be concluded that at a high frequency, stronger electromagnetic coupling between the primary and secondary coils in Design 2 will be expected than that in Design 1; and for Design 2 without PGSs, a similar phenomena can be observed.

Since $G_{\text{max}}$ and $\text{NF}_{\text{min}}$ can be derived from each other, we only give one example, as shown in Fig. 11, to demonstrate the frequency-dependent characteristics of $\text{NF}_{\text{min}}$ of an NPGS transformer Design 1 at different temperatures. It is obvious that $\text{NF}_{\text{min}}$ does not change monotonously with frequency increasing, which is different from that shown in [22]. This is because the frequency range up to 20 GHz is considered here. The implementation of a PGS can improve $\text{NF}_{\text{min}}$, e.g., $\text{NF}_{\text{min}}$ increases by 18%–33% for the $N = 4$ interleave case from 4 to 6 GHz, which is not plotted here.

![Fig. 11. $\text{NF}_{\text{min}}$ of an NPGS transformers of Design 1 versus frequency at different temperatures.](image)

**B. $Q$ Factor**

Based on (4), the frequency- and temperature-dependent $Q_1$ factor of the primary coil of Design 1 with a PGS is extracted with $N = 4$, and the $Q_1$ factor of its NPGS counterpart is also given for comparison, as shown in Figs. 12 and 13.

For Design 1, the following is observed.

1) Although the temperature rise from $T = 253$ K to 333 K causes a significant decrease in $Q_{1,\text{max}}$, such negative temperature effects can be compensated, to some extent, using a PGS with an appropriate embedding depth. It is seen that for the PGS Design 1, $Q_{1,\text{max}}$ at $T = 373$ K is still larger than that of $Q_{1,\text{max}}$ at $T = 298$ K of NPGS Design 1.

2) As indicated in [22], there are also reverse temperature effects, i.e., as frequency exceeds a certain frequency corresponding to the zero temperature coefficient of silicon resistance $R_{\text{b1}}$ and $R_{\text{b2}}$, the $Q_1$ factor increases with temperature. This is because, at higher frequencies, the $Q_1$ factor is dominated by the silicon substrate resistances $R_{\text{b1}}$ and $R_{\text{b2}}$, which exhibits a positive temperature coefficient.

The relative enhancement in the $Q_1$ factor is defined by

$$
\Delta Q_{1,\text{enh}}(T) = \frac{Q_{1,\text{max}}^{(1)}(T) - Q_{1,\text{max}}^{(0)}}{Q_{1,\text{max}}^{(0)}}
$$

and in the case of $N = 4$, $\Delta Q_{1,\text{enh}}(T) = 33.3\%$, 26.2\%, and 20.7\% at $T = 298$, 333, and 373 K, respectively. It is apparent that the decrease in the $Q_1$ factor of Design 1 can be compensated due to the shielding effectiveness of the PGS embedded at the metal layer of M1. However, in the case of Design 2, there is only a slight increase in the curves of the $Q_1$ factor that starts beyond the frequency $f = 2.5$ GHz approximately when the substrate resistance becomes more dominant.

![Fig. 12. $Q_1$ factors of the primary coil of an NPGS transformer of Design 1 versus frequency at different temperatures.](image)

![Fig. 13. $Q_1$ factors of NPGS transformers of Designs 2 versus frequency at different temperatures.](image)
C. Power Loss

Fig. 14 shows the power loss $P_{\text{loss}}$ of NPGS transformer of Design 1 versus frequency at different temperatures, and $P_{\text{loss}}$ is defined as

$$P_{\text{loss}} = 1 - |S_{11}|^2 - |S_{22}|^2.$$  \hfill (27)

It is obvious that the implementation of the PGS can reduce the power loss of the transformer of Design 1 because of its shielding effectiveness. For comparison, Fig. 15 shows the power losses of the NPGS transformer of Design 2 with $N = 3$ versus frequency at temperatures of $T = 253$, 298, 333, and 373 K, respectively. It is observed that for the transformers of Design 2, the implementation of a PGS has little effect on the reduction of power loss.

V. CONCLUSION

Frequency-thermal characterization of on-chip transformers with and without PGSs has been carried out in this paper. These transformers are fabricated using 0.18-µm RF CMOS processes, where the same inner dimension, metal track width, track spacing, and silicon substrate are. The above results demonstrate that there exist significant differences in the performance parameters between interleaved and center-tapped interleaved configurations. The maximum available gains of interleaved transformers at low frequencies are higher than those of their center-tapped counterparts, but at higher frequencies the situation will be reversed. In an environment of relatively high temperature, the thermal effects on the performance degradation of transformers and even other passive devices must be considered carefully. It should also be emphasized that, in order to enhance the shielding effectiveness of a PGS, its embedding depth must be chosen appropriately.

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REFERENCES

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