Impact of Packaging Design on Reliability of Large Die Cu/low-κ (BD) Interconnect


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Abstract

This paper presents the study on the effect of low κ stacked layer, chip pad design structures, and shift pad design of a large die size Cu/low κ (BD™) chip for improving assembly and reliability performance on organic buildup substrate FCBGA (FlipChip Ball Grid Array). Bump shear characterization has been performed on the integrity of different stacked layer and pad structure, supported by bump shear modeling analysis. Initial reliability testing was performed on assembled package to identify the best choice of design and finally implemented on the reliability test vehicle for verification. In addition, a potential chip crack problem due to excessive warpage in FCBGA with large die assembly is examined and a simple failure criterion is proposed.

Introduction

With shrinking of CMOS device, Cu/Low κ interconnection has been adopted in the IC process for the RC delay reduction. And it is moving towards finer technology nodes from 90nm to 65 nm and 45nm. The low κ dielectric is critical in ensuing better capacitance, device speed and signal integrity of the Cu interconnect. However, mechanically the dielectric material has lower modulus, brittle and lower adhesion strength [1,2]. Many works have reported concerns on the mechanical integrity of Cu/low κ chip and its susceptibility to chip failure in reliability testing [2,3,4,5].

On the other hand, Flip Chip package is gaining increased popularity as the preferred solution for high performance ASIC and microprocessor devices, with a trend towards more I/O, finer pitch and larger chip size. For cost consideration, organics substrate has been employed instead of the more expensive ceramic substrate [6,7]. The tradeoff is CTE mismatch between the silicon chip and substrate resulted in larger thermal strain in solder joint. With larger chip size and smaller bump size, the thermal strain in the solder joint is increased with distance from chip center. In addition, the use of higher reflow temperature for Pb free solder process has further aggravated the overall package stress.

The combined effect of large die size, finer bump pitch, Pb free solder packaging on advanced Cu/low κ chip is expected to be more challenging, hence it is imperative to study the chip-package interaction more closely for improving the overall robustness of Cu/low κ package. The chip locations with direct connection and interaction with packaging materials such as the region underneath solder bump are the key interest for investigation. This paper presents the study on the effect of low κ stacked layer, chip pad design structures, and shift pad design of a large die size Cu/low κ (BD) chip for improving assembly and reliability performance on organic buildup substrate FCBGA. Bump shear characterization has been performed to compare mechanical robustness of low κ stacked and pad structures. Bump shear modeling analysis and reliability testing were also performed to identify the best solution and finally implemented on a reliability test vehicle for package level reliability test verification. In addition, a potential chip crack problem encountered in FCBGA with large die assembly has been examined and a simple failure criterion based on maximum bending stress and critical chip strength obtained from 3-point bending test is proposed in the paper.

I) Study on effect of Low K stack

Test sample and characterization

Traditionally Si₃N₄ and SiO₂ have been employed for protecting the metallization and circuitry in the chip. For Cu/low κ chip, some extra layers of passivation may be included for better protection and to act as stress buffer for the Cu/low κ layer underneath the bumps. For this purpose, three different low κ stack structures have been fabricated as shown in Figure 1. The 15 layer structure correspond to the standard 3 metal layer Cu/low κ test device available in our laboratory, hence it is adopted as control. It consisted of 2 stacks of Si₃N₄/USG layer due to process requirement for passivation opening on the metal pad. The other structures represent one stack Si₃N₄/USG short (e.g. 13 layers) and one stack extra (e.g. 18 layers) compared to the standard 15 layers. This means the 18 layers structure has additional 2 layers of 3000Å of USG with one Si₃N₄ on top of the standard 15 layers structure. Presumably these additional passivation layers provide further protection to the low κ stack below it. On the other hand, the 13 layers structure has excluded a 5000 Å USG layer in its passivation hence reducing its cushion effect. A fourth sample with additional polyimide layer on the standard was included represent that of a redistribution layer (RDL). The standard blanket wafer fabrication procedures have been adopted except that there is absent of Cu metallization layer within the low κ stacked layers. For electrical continuity checking purpose, a simple daisy chain was formed using the top Cu electroplated metal layer for a die size of 17.5mm x 17.5 mm, with 150 um bump pitch of 10 peripherals rows. Spin coated
polymer dielectric is formed on the top metal layer followed by electroplated TiW/Cu UBM and Sn2.5Ag solder [8]. The schematic of bumped chip samples are shown in Figure 2.

![Schematic of bumped chip samples](image)

Figure 1: Blanket low $\kappa$ stacked structures

Initial dicing experiment was performed using straight dicing but peeling was encountered in all the samples. Dicing optimization was performed using 2-step process with a 45 degree bevel dicing followed by straight dicing. Optical and SEM inspection on dicing edges confirmed 2-steps dicing without any sign of delamination, see Figure 3. To further confirm the robustness of the 2-step dicing, the dicing water flow rate was increased from the normal 0.5 litre/minute to 1.0 litre/minute while the spindle speed is keeping at 30krpm and table speed at 30mm/sec for process throughputs. Presumably the higher water jet impingement to the dicing edge is worst when water flow rate is increased however the dicing edge quality remained good for all the all samples.

![Dicing quality check of low $\kappa$ stacked wafer](image)

Figure 3: Dicing quality check of low $\kappa$ stacked wafer

After that, the diced chips were subjected bump shear characterization after multiple reflow exposure at peak temperature of 260°C and thermal aging of 150°C for 1000 hours. Shear height was 15um and shear speed 0.05 mm/sec. The results show only bulk solder shear failure for all the 4 types of low $\kappa$ structures. Typical failure modes of the samples are shown in Figure 4. In addition, CSAM (C-Mode Scanning Acoustic Microscopy) was performed on the bump sheared chips to verify if there was any delamination below bump area. Typical of the CSAM images are shown in Figure 5 where no delamination was detected (e.g. in the circled area). These initial chip level characterization results do not show any significant differences among the 4 types of low $\kappa$ structures. Further analysis need to be performed for comparison of them.

![Bump shear failure mode](image)

Figure 4: Bump shear failure mode

![CSAM images on bump sheared sample](image)

Figure 5: CSAM images on bump sheared sample

**Bump shear modeling**

The bump shear test was modeled with FE (Finite Element) method to reveal stresses distribution and the interfacial stresses in the low $\kappa$ stacked layer underneath the bump. 2D plain strain FE model as shown in Figure 6 with shear ram modeled as rigid part without deformation. UBM layer was considered as bilinear plastic, solder as elastic-plastic and the rest of material including the low $\kappa$ stacked layers as elastic material. [9]

Figure 7 shows the peel stress distribution in the structure at 5um shear displacement into the solder. The region directly under the shear ram shows strongest effect. Maximum peel stress is found to occur at top interface of Blok™/BD in the low $\kappa$ structure. In addition to the shear height of 15um, the thickness of UBM has further contributed to the shear distance from shear tip to the low $\kappa$ stack layer below it. The resultant
Reliability test verification

The bumped chip of different passivation structures were assembled by flip chip attached on BU (Build-up) substrate in FCBGA for reliability assessment. After that, the samples were subjected to level 3 Moisture Sensitivity Test (MST L3) with 260°C reflow temperature and Temperature Cycling (TC) test at -40/125°C. Daisy chain continuity measurement was performed before and after reliability test and the failed sample was subjected to CSAM for interfacial delamination check. The results are summarized in Table 2. The 13 layer low κ structure was found to be worst as compared to the thicker layer structures (e.g. 15 and 18 layers). Generally the result agrees with bump shear modeling prediction where higher interfacial stress is occurred on thinner structure except for the 18 layer structure. It seems further increase in low κ passivation thickness has resulted in other negative effect that has led to interfacial delamination. There seems to have a compromise in the passivation thickness for useful application. Based on this reliability results, the 15 layer structure was selected for further use in subsequent study.

II) Study on effect of pad structure

As shown in the FE modeling results, the low κ region underneath the bump has higher interfacial stresses and it is concerned of damage when subjected to assembly or reliability stressing. The questions on whether one can place a bump metal pad which is sitting directly on Cu/low κ structure or one should avoid it is of important to find out for our chip design. Therefore we have also considered different bump pad structure design consideration for ensuing robustness of the low κ structure against bump stress.

Test sample description and characterization

Five different bump pad structures have been fabricated, as shown in Figure 9, all on a 20x20mm Cu/low κ chip with 15 layer stack structure. These include on-pad structure, off-pad structure and off-set pad structure. These pad structure are
located at different places on the same chip (e.g. chip center and chip corner) for comparison (Figure 10). The bump-on-pad structure is presumably the most vulnerable to bump stress damage hence it was used as control. The off-pad structure is to avoid the bump sitting directly on pad. In addition, a distribution RDL with polyimide layer is included for comparison. The off-set pad structure represents a situation where the bump is overlap with metal pad in the Cu/low κ chip. Three stacked Cu pads were connected by the submicron via in this design. Metal pad size is 120um square while the bump pad opening is 60um and UBM is 80um. Solder bumping process and material are similar to what has been described in section (I).

Figure 9: Pad structures under evaluation

a) On pad (with RDL)

b) Off pad (with RDL)

c) Off set pad (with RDL)

d) On pad (without RDL)

e) Off pad (without RDL)

Figure 10: Bumped chip with RDL and pad structures

After dicing, the Sn2.5Ag bumped chips were subjected to multiple reflows at peak temperature of 260°C and bump shear characterization. The summary of shear test results is shown in Table 3. For chip without RDL layer, the off-pad design has bulk solder shear while on-pad design has shown pad peeling failure. In comparison, samples with RDL layer have shown some improvement. The on-pad structure failed only after 3-time reflows exposure while the off-set pad sample failed after 10-time reflows exposure. The off-pad structure performed the best compared to the other pad design and showing only bulk solder failure. Figure 11 shows the failure mode of various pad design. The results show indicate clearly the vulnerability of the Cu/low κ structure below bump area and the importance of avoiding bump to sit directly or overlapping with the current metal pad structure design of the Cu/low κ chip. The presence of polyimide layer does provide some cushioning but it is still insufficient to support direct bump.

Table 3: Summary of bump shear test

<table>
<thead>
<tr>
<th></th>
<th>Without RDL</th>
<th>With RDL</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>On pad</td>
<td>Off pad</td>
</tr>
<tr>
<td>After dicing</td>
<td>×</td>
<td>✓</td>
</tr>
<tr>
<td>3X reflow</td>
<td>×</td>
<td>✓</td>
</tr>
<tr>
<td>10X reflow</td>
<td>×</td>
<td>✓</td>
</tr>
</tbody>
</table>

× failed ✓ passed

Figure 11: Bump shear failure mode of different pad structure

For reliability assessment, the test chip was assembled on a 2-2-2 BU substrate with underfill selected earlier for Cu/low κ application, and the samples were subjected to TC testing. Daisy chain resistance measurement and CSAM have been performed before and after the test. CSAM analysis has revealed pad delamination on the location corresponding to the on-pad and offset pad only. All of the on-pad samples have shown good results without electrical open or delamination. Figure 12 shows a zoom-in CSAM image of the sample with pad delamination as indicated by the brighter spot area on the chip. The corresponding chip layout schematic at the same region is included in Figure 12 for comparison. An excellent match has been observed where all of pad delamination was located at the on-pad or offset pad region.

The bump shear test and TC test on the assembled package have both revealed similar weakness in the pad region for the Cu/low κ chip currently fabricated. The TC test results of the assembled chip match well with bump shear test results where pad peeling has occurred. The low κ chip is particularly weak and it is not able to support solder bump on its pad region (e.g.
on the pad or slightly overlap with the pad). The results indicate that the only way to have solder bump made on the current Cu/low κ chip is to redistribute the bump from the pad region with RDL away from the metal pad. As a result of this experiment, RDL layer was confirmed and added to the Cu/low κ chip for subsequent use. A new bump layout was made to incorporate with RDL redistribution and fabricated on the remaining Cu/low κ device wafer for final package reliability verification.

Figure 12: Chip delamination vs. pad location

**Reliability verification for improved structure**

Due to its susceptibility of the Cu/low κ chip to premature failure, a more compliant solder e.g. high Pb (95Pb/5Sn) was also included in addition to Sn2.5Ag solder. The purpose is to further reduce the interfacial stress in the low κ stack of the chip as shown in bump shear modeling results earlier. Table 4 shows the detail matrix of reliability test vehicle, and a schematic of the FCBGA package is shown in Figure 13.

![Figure 13: Schematic of 20x20mm Cu low κ chip and the FCBGA with 2-2-2 BU substrate](image)

In addition to the low κ stack and pad location, the parametric analysis of the bump pad configuration (e.g. pad thickness, via size, dielectric thickness, etc) has also been investigated using FE modeling and the results were published elsewhere [10]. The final reliability test vehicle has incorporated with all of the desirable parameters for final reliability performance verification.

The summary of the MST and TC test results are shown in Table 5. The results show all of samples passed MST L3 test without daisy chain open failure. However CSAM inspections on the tested samples have revealed chip corner delamination on the high Pb sample with C5 underfill only. Micro-section prepared by using Ar polisher followed by SEM inspection has shown chip corner delamination occurred at both dielectric/underfill and PI/low κ stack interface in Figure 14. For the TC test, all the samples have passed the extended 2000 cycles without daisy chain open failure or CSAM delamination. For verification of solder bump integrity, the reliability tested samples were subjected to cross-section and SEM inspection. All the solder joints are found to be intact without crack (Figure 15). The results have demonstrated that the large die FCBGA with Cu/low κ test chip have achieved good reliability of MST L3 and TC testing without major issues. The cause of underfill delamination found on the C5 underfill in MST test was undetermined even after looking at the underfill evaluation data (e.g. not published here) like hot-wet adhesion test and its stress performance by FE analysis.

### Table 4: Details of Cu/ low κ chip reliability test vehicle

<table>
<thead>
<tr>
<th>Chip type</th>
<th>Cu/low κ, 3 metal layer, 15 stack structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die size</td>
<td>20mm x 20 mm</td>
</tr>
<tr>
<td>Bump pitch</td>
<td>300 μm</td>
</tr>
<tr>
<td>UBM</td>
<td>TiWCu + mini Cu (7um thick), 80um dia.</td>
</tr>
<tr>
<td>RDL</td>
<td>Electroplated Cu</td>
</tr>
<tr>
<td>Solder</td>
<td>Sn2.5Ag, Sn95Pb</td>
</tr>
<tr>
<td>Substrate</td>
<td>2-2-2 BU substrate</td>
</tr>
<tr>
<td>Package size</td>
<td>45mm x 45mm</td>
</tr>
<tr>
<td>SOP</td>
<td>SAC type for SnAg bump, SnPb for high Pb bump</td>
</tr>
<tr>
<td>Flip chip reflow</td>
<td>245°C for SnAg, 225°C for high Pb chip</td>
</tr>
<tr>
<td>Underfill</td>
<td>3 types (N1,N2,C5)</td>
</tr>
<tr>
<td>Reliability test</td>
<td>MST L3, TC –40/125°C @1000 cycles</td>
</tr>
</tbody>
</table>

### Table 5: Reliability verification for improved design

<table>
<thead>
<tr>
<th>Bump solder</th>
<th>UF</th>
<th>S/S</th>
<th>MST L3 (260°C)</th>
<th>TC 2000 cyc</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>ET (open)</td>
<td>CSAM (Delam)</td>
</tr>
<tr>
<td>SnAg</td>
<td>N1</td>
<td>16</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>High Pb</td>
<td>N2</td>
<td>16</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>High Pb</td>
<td>C5</td>
<td>8</td>
<td>3</td>
<td>0</td>
</tr>
</tbody>
</table>

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(III) Study on effect of pad shift design

Due to different CTE (Coefficient of Thermal Expansion) of the organic substrate (e.g. 18 ppm/°C) and silicon chip (e.g. 3 ppm/°C), there is a mismatch of DNP (Distance from Neutral Axis) for the solder bump on the chip and the corresponding metal pad on the substrate during solder reflow process, as illustrated in Figure 16. A die size of 20mm x 20mm will expect to have delta DNP of as much as 40um at melting temperature of 230°C for SAC based solder. For a large die flip chip of 150um bump pitch with 80um pad opening on the substrate, a bump-metal pad mismatch of 40um may stand the risk of bump landing on the solder mask causing non-wetting or cold joint problem during flip chip attach reflow process.

A novel shift pad design is adopted to prevent this problem. The idea is to place the metal pad slightly inwards such that it will match the solder bump as it expands at higher temperature during reflow process, as shown in Figure 17. For this study, a progressive shift pad layout from the neutral point outward to the chip corner has been designed for a 20mm x 20mm Cu/low κ chip with 150um bump pitch. It is possible to work out the temperature for good matching using FE analysis. However for demonstration purpose, the mid point temperature e.g. (230°C – 23°C)/2 is taken as reference as DNP matching temperature. A full compensation design was not used because of the consideration that excessive pad shift may lead to higher residue stress when the assembly is cooled down. And the effect on the shape of the resultant solder joint and its consequence on solder joint reliability. For comparison, sample without pad shift design were also included.

Assembly of the FCBGA samples was done using same process condition for both normal chip and samples with shift pad design. Table 6 shows the assembly yield data after underfill curing. Despite a small sample size, the results show the shift pad design has improvement over the normal chip especially on preventing daisy chain open failure. Cross-section of the open failure have confirmed non-wetting of solder bump on the normal chip (Figure 18). Nevertheless, further assembly process optimization have been carried out by controlling the flux dipping height and flattening of pick up nozzle to ensure good solder joint formation for both chip type. The final assembly has shown good flip chip processability without non-wetting, daisy chain open, underfill voids and delamination problem for all the chips.

Table 6: Assembly yield of flipchip assembly

<table>
<thead>
<tr>
<th>Sample size</th>
<th>Underfill voids</th>
<th>Daisy chain open</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal chip</td>
<td>75</td>
<td>0</td>
</tr>
<tr>
<td>With shift pad design</td>
<td>45</td>
<td>0</td>
</tr>
</tbody>
</table>
After the flip chip assembly, the samples were subjected to MST L3 (reflowed at 260°C) and Temperature cycling at -40/125°C for 1000 cycles. No electrical open failures or CSAM delamination failure were detected on all the samples shown in Table 6. For verification, cross-section was carried out on the outer row solder joint for sample before and after reliability testing for every group followed by SEM inspection. Figure 19 shows SEM image of solder joint quality for each sample after TC 2000 cycles.

Table 7: MST and TC results for shift pad vs. normal sample

<table>
<thead>
<tr>
<th>Bump solder</th>
<th>Pad type</th>
<th>S/S</th>
<th>ET (open)</th>
<th>CSAM Delam</th>
<th>ET (open)</th>
<th>CSAM Delam</th>
</tr>
</thead>
<tbody>
<tr>
<td>SnAg</td>
<td>N</td>
<td>8</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>SnAg</td>
<td>S</td>
<td>8</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>High Pb</td>
<td>N</td>
<td>8</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>High Pb</td>
<td>S</td>
<td>8</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

N = normal  S = shift pad

Cross section of the solder joint revealed that both the shift pad and normal samples show some distortion in the solder joint especially as the solder joint is located further from the chip center. However, the shift pad sample with SnAg solder has less distortion compared to the normal chip sample for both SnAg and high Pb bump samples. Up to TC 2000 cycles, however, there was no failure in both of samples. The solder joint remain in tact without crack. The results suggest that the pad shift design is compatible to the normal chip in MST and TC performance. The current study represents the initial work we have done on pad shift approach for improving assembly yield of large die flipchip. Good feasibility is obtained based on limited samples. Further study with larger samples and further reliability testing is being considered.

Conclusions and Recommendation

The effects of low κ stack layer, chip pad design structures, and shift pad design of a 20x20mm Cu/low κ (BD) chip have been investigated for improving the assembly and reliability performance on organic buildup substrate FCBGA. Some of the important results and recommendation are summarized in the following.

1) FE analysis showed maximum peel stress is occurred at top interface of Blok/BD in the low κ stack structure.
2) The 15-layer low κ stack structure provided best compromise in stress at under bump area and reliability performance for our current Cu/low κ chip.
3) The existing Cu/low κ chip has been shown that it is unable to support direct bump on pad. A redistributed RDL layer with polyimide layer has been employed to ensure the existing chip to survive multiple-reflow test and package reliability test.
4) By combining the best design structures, namely the 15-layer low κ stack and off pad design with RDL, we have successfully demonstrated good assembly and reliability of a FCBGA with 20x20mm Cu/low κ chip.
5) A novel shift pad design has been demonstrated to show improved assembly yield and comparable reliability performance as the normal chip.
6) Removing the USG passivation layer for low κ stack chip has resulted in higher normal and shear under bump area and more reliability failure in MST and TC testing. Thus, it is recommended to keep the USG layer to ensure robustness of the Cu/low κ chip.

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References


