Abstract—This paper is for process development of assembly technologies used to fabricate the 3-D silicon carrier system-in-package (SiP). The five assembly technologies are wafer thinning, thin flip chip attach on silicon carrier, ultra low loop wire bonding, glass cap fabrication and sealing, and silicon carrier stacking. The developed SiP has three silicon carriers with four flip chip and one wire bond die chip attached and the carrier is stacked one above the other to form the 3-D silicon carrier SiP. Eight-inch bumped wafer thinning down to less than 100 μm, lower flip chip interconnect height between the chip and the carrier down to 35 μm, 40–50-μm low loop wire bonding on overhang by direct reverse wire bonding method using 1-mil-diameter Au wire are achieved. And investigation of three types of thin film metallization systems for wirebonding and investigation of two different methods in fabricating glass cap are also studied.

Index Terms—Stacked module, three-dimensional packaging, three-dimensional system-in-package (SiP), through silicon via (TSV).

I. INTRODUCTION

THREE-DIMENSIONAL packaging with through wafer via structure, via fill process, and thinned die packaging is identified as near term assembly and packaging challenges for ≥32 nm in recent ITRS 2006 [1]. Space constrained portable electronic gadgets like hand phones, mini disk drives, MP3 players, digital cameras, and personal digital assistant (PDA) drive 3-D system-in-package (SiP) solution. Many researchers [2], [3] have developed laminate, silicon based 3-D SiPs to achieve high-level miniaturization saving the real estate of the printed circuit board (PCB) and to integrate multifunctional devices and passive components. Among these 3-D packaging technologies, 3-D SiP based on silicon carrier technology is one of the promising candidate taking into consideration of ultra fine pitch wiring, higher thermal conductivity, and thin film/trench capacitor passives integration. Silicon chips on silicon interposers or carriers with integrated function such as decoupling capacitors may provide a better module architecture compared to increased on-chip decoupling or off-chip discrete passives such as capacitors, inductors, and resistors mounted on package at the chip perimeter or underside of the package.

Regarding to through silicon via (TSV) substrate, there is very little literatures and works published. Many papers discussed only TSV interconnection itself (i.e., Cu plating) or substrate-to-substrate interconnection works. Three-dimensional silicon carrier SiP developments have been published earlier [4]. Development of microelectromechanical systems (MEMS) wafer fab processes like KOH silicon etching, silicon deep reactive ion etching (DRIE), deep via Cu plating over the years have enabled manufacturability of silicon carriers/substrates [5], [6] which will be the solution to existing problems in packaging like reliability of ultra fine pitch flip chip interconnects, large die, large input/output (I/O) packaging issues [7], and opens up window for research in 3-D miniaturized electronic modules. We understand this may be first paper describing flipchip and wirebonding interconnections to TSV substrate as well as module assembly.

Major challenge for 3-D silicon stacked module can be described as three items.
1) Chip-to-Si substrate: flip chip and wire bonding.
2) Si substrate-to-Si substrate: intercarrier interconnection.
3) Stacked module assembly: SMT and glass cap attachment, etc.

Especially, chip-to-Si-substrate interconnection and assembly is quite new and needs more research and development works to establish fine pitch interconnection to maximize the advantage of Si substrate technology. The schematic of the 3-D SiP developed is shown in Fig. 1. In this research work 3-D silicon carrier SiP that can integrate one processor in silicon carrier 1, two memory dies in silicon carrier 2, and one flip chip digital signal processor and one wire bond image sensor die in silicon carrier 3 is developed targeting handheld electronic products with imaging application. Reliability studies and thermal performance of the developed 3-D SiP is presented in [8], [9] respectively. This paper addresses the assembly and
process development done in order to build the 3-D silicon carrier SiP for handheld applications.

II. EXPERIMENTAL PROCEDURE

The 3-D silicon carrier SiP developed in this work has silicon carriers with Cu plated through hole interconnect where known good dies (KGD) can be wire bonded or flip chip attached and tested for known good carriers (KGC) and then the KGCs are stacked in the vertical direction to form a module. The 3-D silicon carrier SiP has one 8×8 mm² flip chip with 250-μm pitch attached to silicon carrier 1, two 5×9 mm² flip chip with 200-μm pitch attached to silicon carrier 2, and one 7×7 mm flip chip with 150-μm pitch and on top one 8×8 mm² wire bond die is die attached and wire bonded to silicon carrier 3, glass cap is also attached to silicon carrier 3 to protect the wire bond chip.

Challenges in assembly technologies are as follows:

1) wafer thinning: ultra thinning of 8-in bumped, standard silicon wafer and carrier wafer;
2) flip chip attach;
3) wire bonding: ultra low loop wire bonding on over hang, wedge bonding on thin film metallization;
4) glass cap fabrication and sealing: glass fabrication method using MEMS technology, void free and adhesive displacement free cap sealing process;
5) carrier stacking: carrier bumping and controlled inter carrier stand off.

A. Silicon Carrier Fabrication

13.5×13.5 mm² size silicon carriers with through hole interconnects are fabricated in a 8-in silicon by through hole via micromachining of by DRIE, via isolation, seed layer sputtering, support wafer bonding, Cu electroplating to fill the vias and support wafer debonding. The detailed through via processes are described and discussed in previous work [5]. The silicon carrier fabricated has under bump metallization (UBM) pads for flip chip attach and the same metallization for wire bond interconnection of image sensor die to the silicon carrier. Top side of the carrier wafer metallization is done with two-layer metallization and two-layer SiO₂ process for the bottom side of the carrier wafer the through hole via copper is plated with electroless nickel immersion gold (ENIG) for solder wet ability.

B. Test Die Fabrication

Flip chip test chip 1, 2, 3, and 4 are fabricated with Al metallization deposition on SiO₂ layer, Al patterning followed by passivation with SiO₂/SiN deposition and patterning and finally ENIG UBM deposition. Ashai Sunfort YQ-50 Dry film is laminated onto the wafer and photolithography is done using suitable mask. Developing the dry film leaves cavities on top of the UBM for solder paste printing. Lead free solder paste type 6 (Sn-3.5Ag-0.5Cu from Heraus, Saint Paul, MN) is selected for paste printing on the developed dry film. Solder paste printing is carried out followed by lead free reflow to form solder bumps. Optical inspection of the bumps is done to measure the solder bump height and the bumps are inspected in X-ray machine to analyze for any voids in the solder bumps. After lead free bumping bump shear is done to qualify the bumping process. Shear test reveals solder bump cohesive failure mode which proves that the adhesion of the UBM and wettability of bump to the UBM is good. X-ray inspection (Dage XDG500) of the bumped wafer shows void free bumping.

Wire bond test chip 5 is fabricated with Al metallization on silicon dioxide (SiO₂) layer and Al patterning followed by passivation with combination of SiO₂ and silicon nitride. Test chips 1, 2, 3, 4, 5 details are given below in Table I.

III. RESULTS AND DISCUSSION

A. Wafer Thinning

The wire bond and flip chip test wafers are thinned by mechanical back grind (BG) and polishing machine. Suitable back grind tapes for wire bond and flip chip test wafers are selected and BG tapes are laminated using a laminator. BG and polishing process parameters are optimized for the target 100 μm thinning of wire bond and flip chip test wafers. The details of process in bumped wafer thinning are discussed in previous work [10]. Suitable ultraviolet (UV) based BG tape is selected for bumped flip chip and wire bond test wafer thinning experiments. The BG tape selected has base film thickness of 100 μm and adhesive/cushioning layer thickness of 150 μm for bumped wafer thinning and 250-μm base film thickness with 70-μm adhesive layer thickness is selected for wire bond wafer thinning process. Void free lamination process is achieved by using required roller pressure and feed speed of the tape. Mechanical BG and polishing is done to thin the bumped wafer from 750 μm to final thickness of 100 μm. Coarse grind using #320 grit till 120-μm wafer thickness followed by fine grind using #2000 grit up to 102 μm and final 2 μm removal by slurry wet polishing is done to achieve 100 μm final thickness. Total thickness variation (TTV) across the wafer using 69 points measurement is done using FSM 413 model that works on the principle of laser to measure the silicon thickness. A TTV of ±4 μm is achieved for bumped flip chip and wire bond test wafers thinned down to 100 μm.

B. Flip Chip And Die Attach Process

The thinned flip chip die is then diced and attached to the silicon carrier 1,2,3 using standard flip chip attach process by
TABLE II
DETAILS OF THE THICKNESS OF METAL SYSTEMS USED IN WIREBONDING STUDY ON SILICON CARRIERS

<table>
<thead>
<tr>
<th>Metal systems</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Ti (0.1µm) / Ni (0.5µm) / Au (0.1µm)</td>
<td></td>
</tr>
<tr>
<td>2 Ti (0.1µm) / Ni (0.5µm) / Au (0.3µm)</td>
<td></td>
</tr>
<tr>
<td>3 ENIG - Ni (3 to 4µm) / Au (0.1µm)</td>
<td></td>
</tr>
</tbody>
</table>

FC150, Karl Suss flipchip bonder—flux dipping, fiducial mark alignment, flip chip attach, and reflow. Dicing-die-attach-film (DDAF) process is evaluated to attach the wire bond die on top of the flip chip die in silicon carrier. The thinned wire bond wafer with the BG tape is laminated with the DDAF using the wafer ring. After lamination the BG tape is removed from the thinned wafer followed by dicing the dies and attaching the wire bond die on top of the flip chip die. Thinned bumped wafer is diced into test chip 1, 2, 3, 4 followed by flip chip attach to the respective silicon carriers. Die shear is carried out to observe the failure location after flip chip attach process. Die shear reveals fracture of the thin silicon die, so unthinned bumped chip is attached to the carrier and die shear test is repeated. Die shear test reveals cohesive solder failure in the chip side. Thinned wire bond test chip 5 is die attached on top of the flip chip test chip 4 using the DDAF (dicing die attach film), followed by die attach curing.

C. Wire Bonding Process

Key focus on wire bond process development includes the following.

1) Wire looping: Short (0.3 mm) and low wire loop height by forward loop wire bonding and direct reverse wire bonding on ENIG plated Al pad process development.

2) Wedge metallization: three types of wedge bond metallization evaluation of different pad metal systems as shown in Table II, Ti/Ni/Au (0.1 µm), Ti/Ni/Au (0.3 µm), and ENIG.

3) Optimization of first bond, second bond parameters to achieve shear strength and pull strength criteria and desired failure mode during ball shear and wire pull tests.

4) Perform high temperature storage reliability study to assess the wire bond integrity of the interconnect.

Wire bonding trials are done using 1.0-mil Au wire in ASM Eagle 60 fine pitch wire bonder. Optical microscope is used to measure the loop height during initial process parameter optimization and finally scanning electron microscopy (SEM) is used to measure the exact loop height. Standard ball shear and wire pull tester is used to determine the ball shear and wedge pull strength following the JEDEC EIA/JESD22-116 and ASTM F459-84 (1995) standards, respectively. Low loop wire bonding on over hang with wire bond test chip on top of flip chip test chip without underfill and wedge on thin film metallization are the challenges encountered in the wire bond process development. Extensive first bond optimization to wire bond on over hang die, looping parameter optimization to achieve low loop height and second bond parameter optimization to place wedge on thin film metallization are carried out to successfully perform the wire bonding. In this section, looping parameter and second bond optimization are discussed in detail.

Design of experiment (DOE) is done to optimize the looping parameter to get the lowest loop profile at the same time to maintain enough clearance between the die edge and the bonded gold wire. Different looping modes in the automatic gold wire bonder are extensively studied to get the minimum loop height.

1) Forward loop wire bonding: In order to optimize the looping parameter, silicon carrier with test chip 4 flip chip attached and test chip 5 die attached on test chip 4 is fabricated. The test chip 5 metallization is Al and the Si carrier metallization is thin film Ti/Ni/Au. First bond is made on the test chip 5 with 0.5 mm overhang on all sides; second bond is made on thin film UBM in the silicon carrier. Low loop by forward loop wire bonding is done by looping process parameter optimization to achieve a bell shape loop. Additional kink is added in the loop parameter as to press the wire without stressing the heat affected zone and at the same time achieve low loop height of 50–60–µm, as shown in Fig. 2.

2) Direct reverse wire bonding: Reverse wire bonding directly on Al metallization is not feasible and hence traditionally additional stud gold bump is placed prior to placing the wedge. The gold stud bump acts as a cushioning layer to absorb the wedge bond force and ultrasonic energy. Direct reverse wire bonding is feasible if a bondable metallization like ENIG is introduced on Al [11]. Test chip 5 with Al metallization is plated with 3–4 µm of Ni followed by 0.1 µm of gold. Direct reverse wire bonding by placing the first bond on thin film metallization in the silicon carrier and second bond on ENIG plated test chip 5 is attempted. In this method the test chip is plated with ENIG. ENIG metallization acts as a platform for directly placing the wedge on the chip.
The ENIG process is done in wafer scale and eliminates the stud bumping process and hence improves the productivity of the wire bonder. By this method after loop parameter optimization a loop height of 40–50 μm is achieved, as shown in Fig. 3.

In direct reverse wire bonding method the test chip metallization is ENIG Ni (3 to 4 μm)/Au(0.1 μm) and first bond metallization is thin film UBM in the silicon carrier Ti (0.1 μm)/Ni(0.5 μm)/Au(0.1 μm). First bond parameter optimization is done for both methods to meet the shear strength requirement. Shear strength, failure mode, and metal remain after shear test are taken as response. Second bond parameter optimization is done to meet the requirements of pull strength. Pull strength, failure mode, and metal remains after pull are taken as responses. Pull test is done at the midspan of the wire length following the ASTM F459-84(1995) standard. Second bond force and power are optimized with bond temperature 150 °C, bond time and second bond wedge compensation kept constant. Wire pull is measured for every change in force and power parameters until the desired pull strength and desired pull failure mode is achieved. Also during second bond process parameter optimization the damages onto the underlying SiO₂ is investigated by etching the UBM with suitable chemicals and inspection in optical microscope and SEM.

First bond process parameter is optimized for 100-μm thin and 0.5-mm overhang die until desired ball shear values and failure mode is achieved. Second bonding parameter optimization is done for three types of metal system. Initial experiments with Ti/Ni/Au (0.1 μm) showed tearing of bottom SiO₂ layer after Au/Ni/Ti etching using suitable wet chemicals as shown in Fig. 4. Further second bond parameter optimization is done to eliminate the SiO₂ damages and to meet the wire pull & failure mode requirements. Other two bonding pad systems Ti/Ni/Au (0.3 μm) and ENIG showed no damages to the bottom SiO₂. Wire break failure mode near the neck is observed for the sputtered metalsystems and wire break near the wedge is observed for the ENIG metallization, as shown in Fig. 5. Table III summarizes the wire pull test data for the three types of bonding pad metal systems.

In direct reverse wire bonding first bond parameter is optimized to place the ball on the Ti/Ni/Au (0.1 μm) UBM and second bond parameter is optimized to place the wedge directly on the ENIG metallization plated on Al bond pad. And overhang of 0.5 mm gives additional challenges to wedge bonding process parameter optimization. Fig. 6 shows the picture of wire break failure mode during wire pull test using optimized parameter and Table IV summarizes the wire pull data. After direct reverse wire bonding the ENIG and Al metallization is etched using suitable chemistry and the bond pad is analyzed for damages to SiO₂ layer and no damage to SiO₂ layer is found, as shown in Fig. 7.
TABLE IV
WIRE PULL DATA DIRECT REVERSE WIRE BONDING

<table>
<thead>
<tr>
<th>Pull strength (gm-f)</th>
<th>Min</th>
<th>12.68</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Max</td>
<td>16.38</td>
</tr>
<tr>
<td></td>
<td>Avg</td>
<td>14.83 (+/-2.32)</td>
</tr>
</tbody>
</table>

(a) chip side and (b) silicon substrate side. (Ti/Ni/Au 0.1 μm).

Fig. 7. Optical micrograph of the bond pads with no wirebonding damage in the SiO₂ layer after ENIG and Al metallization etching: (a) chip side and (b) silicon substrate side. (Ti/Ni/Au 0.1 μm).

Fig. 8. Plot of the wire pull strength with time up to 1000 h in HTS.

The wire bonded samples by forward loop wire bonding with three different types of wedge metallization and direct reverse wire bonded samples using optimized wire bond process parameter are subjected to high temperature storage (HTS) reliability test at 150°C for 1000 h in air. As a measure of performance of the interconnect system wire pull test is and the wire pull strength trend over the period of reliability testing is observed. Wire pull test shows no degradation in wire pull strength tested at every 200 h interval as shown in Fig. 8.

D. Glass Cap Fabrication

Glass cap fabrication involves fabrication of silicon window followed by glass wafer bonding by anodic bonding or using UV adhesive. The silicon window thickness is determined by the solder collapse height, flip chip thickness, DDAF thickness, wire bond chip thickness, wire loop height, and the loop to glass clearance. The silicon window is fabricated by DRIE process. 750-μm thick silicon wafer with SiO₂ as hard mask is coated with 10 μm of photo-resist followed by lithography process with suitable mask. After developing resist in the 10 × 10 mm square is opened followed by SiO₂ etching and silicon is exposed. The wafer with developed resist and etched SiO₂ goes through the DRIE process and cavity is machined for a depth of 320 μm. After DRIE process the photo-resist is removed using photo-resist stripper and SiO₂ hard mask is dry etched using plasma. BG is done to remove 430 μm of silicon thickness to form silicon windows in the wafer. Following this a glass wafer is anodic bonded or bonded with UV adhesive to the silicon window wafer. Dicing of silicon and glass wafer is done to singulate individual glass caps. The side view and process sequence for silicon-glass anodic bonded and silicon-glass UV adhesive bonded glass cap are shown in Fig. 9.

Glass cap sealing process is done with adhesives to bond the glass cap with silicon window to the silicon carrier 3 with flip chip and wire bonded chips. Low-temperature cure adhesive is selected for this purpose and is dispensed along the periphery of the silicon carrier three followed by pick and place of glass cap for bonding. After bonding, the silicon carrier with glass cap is placed in the thermal oven for curing at the recommended temperature and timing.

Both Si-Glass anodic bond and Si-Glass UV adhesive bond cap are manufactured at wafer scale, hence its is cheap and batch manufacturable process. In Si-Glass anodic bond cap the glass thickness is limited to 500-μm glass wafer, since thin glass for anodic bonding is not available due to high pressure and process issues during wafer-to-wafer bonding process. However, in Si-Glass UV adhesive cap thin glass wafers can be bonded to make the profile of the package thinner. The fabricated 8-in silicon-glass bonding cap wafer after backgrindning and polishing is shown in Fig. 10.

Die shear test performed to test the adhesion between the interface in both the glass cap reveals mostly glass failure as shown in Fig. 11. At first crack is initiated at the interface but finally failure is happened at bottom glass as shown in failure mode pictures of Fig. 11(b) and (c). This shows that the bonding in the interface is of good quality. The average shear strength is 79.32 Kgf for anodic bonding and 33.48 Kgf for UV adhesive bonding. It is expected that Si-glass anodic bond to be stronger than Si-glass UV adhesive bond due to the permanent bonding between Si and glass. So the difference in shear strength between the two methods is attributed to the bonding nature of different materials set for each bonding.

E. Glass Cap Sealing

Initial trials using thermal cure adhesive shows adhesives are subjected to high temperature storage (HTS) reliability test at 150°C for 1000 h in air. As a measure of performance of the interconnect system wire pull test is and the wire pull strength trend over the period of reliability testing is observed. Wire pull test shows no degradation in wire pull strength tested at every 200 h interval as shown in Fig. 8.

Fig. 11. Reinforced glass cap with silicon window to the silicon carrier 3 with flip chip and wire bonded chips. Low-temperature cure adhesive is selected for this purpose and is dispensed along the periphery of the silicon carrier three followed by pick and place of glass cap for bonding. After bonding, the silicon carrier with glass cap is placed in the thermal oven for curing at the recommended temperature and timing.

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Fig. 9. Optical micrographs of side view of glass caps. (a) Glass anodic bond cap and (b) silicon–glass UV adhesive cap. (c) process flow for the fabrication of glass caps.

Fig. 10. Photo of 8-in silicon-glass bonding cap wafer.

$1.95 \pm 0.13 \times 10^{-7}$ atm cc/s He was acquired. So it passed the near hermeticity test requirement in this study.

F. Carrier Bumping and Stacking

Silicon carriers have three rows of depopulated through-hole interconnects placed at 0.5-mm pitch along its periphery. Carrier bumping is carried out in die level, however can be done in wafer level too. A mechanical jig is fabricated to hold five diced silicon carrier using vacuum and has provision for placing the stencil for solder paste printing and ball placement. Type 6 (particle size 5–15 µm) solder paste is used for solder paste printing followed by 300-µm eutectic solder ball placement using the designed jig. After solder ball placement the stencil is removed.

Fig. 11. (a) Schematics of glass cap shear test and optical micrographs of failure mode after shear test. (b) Si–Glass anodic bond cap and (c) Si–Glass UV adhesive cap.
Fig. 12. Optical micrograph of glass cap sealing using room temperature cure adhesive with wire bond test die seen through the silicon–glass UV adhesive cap.

Fig. 13. Schematics and optical micrographs of two types of glass cap sealed with room temperature cure adhesive on silicon carrier 3.

Fig. 14. Optical micrographs of carrier bumping process: (a) solder paste printing, (b) ball placement, (c) after reflow, and (d) ball placement jig.

and the silicon carrier with solder ball goes through the reflow process. Fig. 14 shows the carrier bumping process.

In carrier bumping the coplanarity of the bumping process is mainly affected by the coplanarity of the Cu filling in the via across the carrier wafer. Solder paste printing to some extent will minimize the bump height variation from carrier to carrier. Bump shear test shows cohesive solder failure and X-Ray inspection of the bumps shows void trapping in case of carriers that have incomplete Cu filling in the through hole via.

In stacking process for assembly of the 3-D silicon carrier SiP, the KGC 1 is first placed onto the PCB, reflowed and followed by underfill process, then KGC 2 is placed on top of KGC 1 reflowed and finally KGC 3 with glass cap is attached to KGC 2. Final assembled of 3-D silicon carrier SiP with glass cap attachment is shown in Fig. 15. Cross section of the 3-D silicon
carrier SiP with Cu through via interconnection with solder is shown in Fig. 16. After completion of assembly and packaging, overall height of 2.2–2.4 mm 3-D silicon carrier SiP is achieved with three silicon carriers and five test chips with glass cap.

IV. CONCLUSION

Five key assembly technologies for fabricating 3-D silicon carrier SiP with its challenges and process optimization are discussed in detail. Wafer thinning is one of the important processes that will determine the overall 3-D silicon carrier SiP thickness. In forward loop wire bonding three types of UBM metallization for wedge bonding in silicon carrier is evaluated and 0.3-mm short loop with loop height of 50–60 μm is also demonstrated without degradation in wire pull strength for 1000-h HTS test. Advantages and processes for direct reverse wire bonding method is discussed and 40–50 μm loop height is demonstrated with 1000 h HTS test validated. Processes for fabricating glass cap by Si-glass anodic bond cap and Si-glass UV adhesive cap is developed and shows the near hermeticity performance after sealing test. Target overall module height of 2.2–2.4 mm is achieved by thinning bumped wafers to 100 μm, low profile flip chip interconnect down to 35 μm, low loop wire bonding to 40–50 μm, selecting thin profile Si–glass UV adhesive cap and controlling the intercarrier stand off height.

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Seung Wook Yoon received the Ph.D. degree in materials science and engineering from KAIST, Daejeon, Korea, in 1998.

He is Deputy Laboratory Director of Microsystem, Module and Components Laboratory, Institute of Microelectronics (IME), Singapore. He has been at IME since 2002 with his major interest in the fields of Cu/low-k/ultra low-k packaging, TSV technology, 3-D silicon technology, wafer-level integration, and microsystem packaging. Prior to joining IME, he was member of technical staff position for advanced electronic packaging and module development at Hynix Semiconductor from 1998. He has over 90 journal papers and conference papers and several U.S. patents on microelectronic materials and microsystem packaging.

V. P. Ganesh received the B.Eng. in mechanical engineering from Bharathiar University, India.

He is a researcher from a materials, process, and assembly background working in the Microsystems Modules and Components Laboratory at Institute Of Microelectronics (IME) Singapore. He has been involved in wafer thinning process development and process integration for 3D SiPs. His research focus includes Cu/low-K device packaging, large wafer ultra thinning and development of 3-D SiP based on silicon platform.

Samuel Yak Long Lim received a degree in mechanical and manufacturing (honours) from the University of South Australia and a diploma in mechatronics from Temasek Polytechnic, Singapore.

He is a Laboratory Officer in Institute of Microelectronics (IME) under the Microsystems, Modules and Components Laboratory. His main interest is in developing low-cost packaging processes.

Vaidyanathan Kripesh received the Ph.D. degree from Max-Planck Institute, Stuttgart, Germany.

He has a wide experience in packaging industry for the last 18 years. He is presently a Senior Member of Technical Staff at Institute of Microelectronics, Singapore, heading a group of researchers in 3-D-stacked module, wafer-level packaging, and guided self assembly processes. He holds a Adjunct Faculty position at National University of Singapore (NUS), where he is teaching microelectronics packaging for graduate students. He also provides a short course at leading conferences such as EPTC, etc., and also to in house staffs in flip chip packaging, has 15 international patents and more than 75 publication to his credit. He has delivered more than 28 invited talks and chaired various international conferences.

Dr. Kripesh is the President on International Microelectronics Packaging Society (IMAPS), Singapore chapter.