Abstract
We report the process evaluation and integration for the embedded RF passive device in this paper. Two sets of test vehicle were designed and fabricated for the evaluation of RF passive devices embedded in USG (undoped silicate glass) and BCB (Benzocylcobutene) dielectric. We encountered resistor uniformity issue and BCB capacitor limitation during the process set up. After process issue solving and final platform setting, resistor, capacitor, inductor and bandpass filter were integrated and the high performance functions were demonstrated.

Introduction
With shrinking of CMOS device, total size of the device is expected to shrink also, but more and more function blocks need to be integrated together for the more advance functions. One way is to integrate more devices within or after CMOS device, such as RF passive device. Another way is to package more function blocks together. Both methods target to reduce space and increase function. BCB is a matured material used in packaging [1]. The BCB integration for the RF passive device has attracted a lot of interest [2, 3, 4]. Our works focus on the process development and integration of resistor, capacitor, inductor and bandpass filter for wireless local area network (WLAN) application.

Platform of the RF Passive Device
The RF passive resistor, capacitor, inductor and bandpass filter were integrated by the Cu/USG and BCB after process development and evaluation. The schematic of the final resistor, capacitor and inductor is shown in Fig.1.

Resistor integration and uniformity issue
Fig.2 shows the design of resistors. After TaN deposition and patterning, M1 Cu pads were defined and connected to the TaN resistors. The connection length of TaN and Cu pad is 10µm. The widths of TaN resistor are 10, 20 and 50 µm and lengths are equal to 1, 5 and 10 times of widths.

Resistor integration and uniformity issue
Fig.2. The design of TaN resistor.

The SEM and optical images of resistors are shown in Fig.3 after M1 dielectric etching and M1 CuCMP.

Fig.3. The SEM and optical images at different stages. (a) after M1 etch. (b) enlarged view of (a), (c) top view of the resistors after M1CuCMP.

From Fig.3a and 3b, we can see that the M1 dielectric is fully opened and the TaN resistor connection area was exposed. This will give good connection between M1 Cu pad and the TaN resistor. Fig.3c shows the top view of resistors after M1CuCMP.
Resistances of different resistors within 4 dies (distributed in the whole wafer) were measured by the multimeter after M1CuCMP. The results are shown in the table 1. Resistors near wafer edge have higher resistance. Within the same die, resistances of resistors with different width and length are quite consistent. After analysis, it is noted that the smaller resistors are more sensitive to process variation. The maximum variation of resistance is 25% within the same structure. The big resistance variation will affect the design and performance of RF passive device. A big variation issue was found in the first wafer.

To solve the issue, the CD (Critical Dimension) of the resistor and TaN film were studied. The minimum CDs (10µm) of resistors after mask and etch were measured (9 points per wafer). Good distributions were seen in Fig.4. The CD’s variations of resistors after mask and etch are both within 2%. So the dimension of TaN resistor is not the reason for the big resistance variation in the first wafer.

Fig.4. The CDs of TaN resistor after mask and etch.

To solve the issue, TaN film property was further studied subsequently. One blank wafer was deposited 1KÅ TaN and sheet resistances (49 points) were measured. Fig.5 shows the sheet resistance distribution trend in the wafer map.

Fig.5. The sheet resistance distribution in the wafer map.

The measurement result shows the sheet resistance change from 22.947 to 27.887 Ohm/square respect to center and edge. The maximum variation is 21.5% within the wafer. The wafer edge has higher sheet resistance, which match with the big resistance variation issue.

To solve this issue, we changed the deposition machine from Endura (self induced plasma, deposition rate: 29.76A/sec) to Anewa (Low power, low temperature, deposition rate: 1.26A/sec). After TaN deposition process move to Anewa, we measured the sheet resistance again on the blank wafer with new TaN film. The sheet resistance of TaN film changed from 23.295 to 23.489 Ohm/square within the wafer. The comparison of sheet resistance variation on both deposition processes is shown in Fig.6.

Fig.6. The sheet resistance distributions for the different TaN films.

Table 1. The resistances summary in the first wafer.

<table>
<thead>
<tr>
<th>Width(µm)</th>
<th>10</th>
<th>50</th>
<th>100</th>
<th>20</th>
<th>100</th>
<th>200</th>
<th>50</th>
<th>250</th>
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<tr>
<td>Die A (Ω)</td>
<td>27</td>
<td>127</td>
<td>258</td>
<td>26</td>
<td>120.5</td>
<td>256</td>
<td>25.5</td>
<td>125.5</td>
<td>251.5</td>
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<tr>
<td>Die B (Ω)</td>
<td>26</td>
<td>128</td>
<td>251</td>
<td>26</td>
<td>126</td>
<td>250.5</td>
<td>25.5</td>
<td>125</td>
<td>249.5</td>
</tr>
<tr>
<td>Die C (Ω)</td>
<td>32</td>
<td>153</td>
<td>301.5</td>
<td>32.5</td>
<td>152</td>
<td>300.5</td>
<td>30.5</td>
<td>151</td>
<td>300</td>
</tr>
<tr>
<td>Die D (Ω)</td>
<td>30</td>
<td>140</td>
<td>276</td>
<td>28.5</td>
<td>140</td>
<td>279</td>
<td>28</td>
<td>140</td>
<td>287</td>
</tr>
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Table 2. The resistances summary after process improvement.

<table>
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<th>Width(µm)</th>
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<th>50</th>
<th>100</th>
<th>20</th>
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<tr>
<td>Die A (Ω)</td>
<td>28.4</td>
<td>135.5</td>
<td>269.2</td>
<td>27.8</td>
<td>135.8</td>
<td>270.2</td>
<td>27.3</td>
<td>135.7</td>
<td>269.2</td>
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<td>28.5</td>
<td>135.7</td>
<td>269.6</td>
<td>27.5</td>
<td>135.1</td>
<td>269.7</td>
<td>27.5</td>
<td>135.1</td>
<td>269.7</td>
</tr>
<tr>
<td>Die C (Ω)</td>
<td>28.5</td>
<td>136</td>
<td>270.2</td>
<td>27.8</td>
<td>135.7</td>
<td>270.5</td>
<td>27.4</td>
<td>135.5</td>
<td>270.6</td>
</tr>
<tr>
<td>Die D (Ω)</td>
<td>28.5</td>
<td>136.1</td>
<td>270.2</td>
<td>27.8</td>
<td>135.6</td>
<td>270</td>
<td>27.6</td>
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<td>270.3</td>
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<tr>
<td>Die E (Ω)</td>
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<td>136.8</td>
<td>270.1</td>
<td>27.9</td>
<td>135.6</td>
<td>270.3</td>
<td>27.4</td>
<td>135.4</td>
<td>270.4</td>
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<tr>
<td>Die F (Ω)</td>
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<td>135.7</td>
<td>269.9</td>
<td>27.4</td>
<td>135.2</td>
<td>269.9</td>
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Max variation % | 0.7 | 0.4 | 0.4 | 2.1 | 0.6 | 0.3 | 1.1 | 0.4 | 0.5 |

After deposition process change, maximum resistance variations of measured resistors are within 2.1%. The big resistance variation issue was thus solved.

Capacitor Process and Cu Roughness

The Capacitors embedded in the BCB and USG dielectric were evaluated for the capacitor integration after resistor process development. The basic design of RF capacitor embedded in the BCB dielectric is shown in Fig.7.

Fig.7. (a) the design of capacitor. (b) the open pad de-embedded structure.
M2). Via23 and M3 are used for the final RF capacitor testing connection. Fig.7b shows the RF capacitor open pad de-embedding structure. The BCB capacitor process evaluation was conducted after capacitor design and mask fabrication. 2KÅ Ti and 1.5KÅ Cu seed were sputtered on the 8 inch wafer after buffer layer 8KÅ USG and 500Å SiN were deposited, M1 Cu plate’s pattern was masked, conduct electrical plating, photoresist removal and Cu seed and barrier layer etched back. The process of M1 Cu plated was completed. SiN was deposited, masked and etched for the capacitor dielectric. Capacitor top plate process is same as that of the bottom plate. The photo BCB is coated and exposed Via23 pattern for the inductor integration. The top view and cross-section of capacitor with 500Å SiN dielectric after Cu top plate process is shown in Fig.8.

Fig.8 The top view and cross-section of capacitor after top plate process. (a) top view of capacitor, (b) cross-section of capacitor. (c) Enlarged view of (b).

The full view of capacitor can be seen in Fig.8a. The profile of capacitor can be seen from Fig.8b. Fig. 8c shows weak points of this process. We can observe rough surface on the bottom Cu plates from Fig.8c. The rough surface is caused by the exclusion of Cu CMP on thicker Cu plate process. Also shown is the undercut at the corner of M1 plate resulting from M1 seed and barrier metal etching back after M1 Cu plate electrical plating. This undercut can be reduced, but cannot be prevented because etching back is wet etch process. It was found that the 500Å SiN does not have a good coverage at the corner and vertical area on M1 plate that cause electrical shorting between the two Cu plates. The rough surface and the corner of bottom Cu plate can cause poor coverage within the SiN capacitor dielectric deposition. The roughness of bottom Cu plate is around 43nm in atomic force microscope (AFM) result. We can not change the Cu roughness under current process condition. In order to reduce the Cu roughness impact, SiN dielectric thicknesses splits (Range from 500Å to3KÅ) were done for the performance evaluation. Capacitors were found to be electrically shorted from the tested result on the 1KÅ SiN deposition capacitors. For the capacitors with 1.5KÅ SiN, we got the reasonable electrical results after top Cu plate metallization as shown in Fig.9.

Fig.9. The testing results of different sizes of capacitor with 1.5KÅ SiN dielectric. (a) Capacitors testing after top metal plate process. (b) C-V curves of capacitors. (c). I-V curves of capacitors.

Fig.9a shows the electrical testing after top Cu plate metallization. We can see that Cu surface of the top plate and bottom plate is quite rough. That is the limitation of this process. The C-V curves show all the capacitors are well functional for different size capacitors with 1.5KÅ SiN deposition in Fig.9b. The good performances for different size capacitors are shown in the I-V curves of Fig.9c. After electrical testing, we checked the physical performance of capacitor at the weak point that is shown in the Fig.10. Fig.10(b) and (c) show good coverage of the SiN at the corner of M1 and the vertical area. The undercut at M1 bottom still can be seen in Fig.10(c).
Further test using 2KÅ and 3KÅ SiN capacitor also shows good electrical results. SiN thickness increasing causes a drop in the capacitance. The split results show that the minimum thickness of capacitor dielectric is 1.5KÅ. Below this thickness, there will be capacitor electrically shortening risk.

We integrated the capacitor embedded in the USG dielectric because of BCB capacitor limitation. The Cu roughness, corner and metal undercut effect can be solved by the Cu CMP in damascene process of the capacitor embedded in USG. The design of different sizes of capacitor embedded in USG is similar with BCB capacitor in the Fig.7. But the fabrication process is totally different. The top and bottom plates of capacitor embedded in USG are fabricated with Cu single damascene process. The SiN dielectric of capacitor is protected by the Ta capping layer. SiN film under Ta don’t have any top metal damascene process effect, SiN film can keep good performance for the capacitor. The Cu CMP in the damascene process can reduce the surface roughness of Cu plate so that smooth surface was provided to the further process of inductor. The final structure and cross-section of capacitor embedded in USG are shown in Fig.11.

760Å SiN is successfully integrated in the capacitor shown in Fig. 11b. Top and bottom plates are smooth compared with the plates of BCB capacitor. Fig.11a shows the top view of capacitor after final process. On the left side is RF capacitor and on the right side is the RF open pad de-embedded structure in the Fig.11a. The RF capacitors within 6 dies distributed in the wafer are measured and shown in table 3.

Table 3. The capacitor summary extracted at 2.5 GHz.

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<tr>
<td>Capacitor1</td>
<td>2.39</td>
<td>2.4</td>
<td>2.4</td>
<td>2.34</td>
<td>2.37</td>
</tr>
<tr>
<td>Capacitor2</td>
<td>0.8181</td>
<td>0.8204</td>
<td>0.8281</td>
<td>0.8354</td>
<td>0.8346</td>
</tr>
<tr>
<td>Capacitor3</td>
<td>5.84</td>
<td>5.96</td>
<td>5.98</td>
<td>5.97</td>
<td>5.97</td>
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Maximum variation of measured capacitor in the wafer is 3% at extracted 2.5GHz in the table 3. That can be used in the further bandpass filter integration.

Compared BCB and USG capacitor processes, we found capacitor embedded in the BCB have limitations. Such as, bottom Cu plate’s roughness and corner affect on the SiN coverage, top Cu plate roughness’s affect the inductor via open. Metal undercut in top and bottom metal plates cannot be prevented by the Cu seed and barrier layer wet etch back process after Cu electrical plating. Advantage of this process is cheap, save the process time and lower capacitance requirement. For the USG capacitor process, that can prevent these limitation, but the process is expensive. For the demonstration of high performance RF passive device, we choose capacitor embedded in USG as the final test vehicle process.

High Performance Inductor and Filter

Inductors embedded in BCB and USG dielectric were reported in [6]. Photo BCB was selected as via and top metal dielectric in this paper because 10µm depth via and 10 µm thick Cu trace were required for the high inductor performance that is difficult to be fabricated by conventional Cu damascene process. 0.72 and 0.81nH at 2.5GHz inductors are designed and fabricated as shown in Fig.12.

Fig.12 The inductor (a) and open pad de-embedded structure (b) after full process.

The inductors were fabricated on the top 2µm Cu plate of capacitor. 2µm Cu line embedded in USG is used as the underpass of inductor. 10µm photo BCB patterned the via, 2KÅ Ti barrier and 1.5KÅ Cu seed layer were sputtered, top metal trace of inductor was masked by 13µm photoresist, electrical plating of 10µm Cu trace and 10µm depth via was conducted. After photoresist removal, Cu seed and barrier metal was wet etched back to form via and top metal trace of
inductor in the same process. Last was the top dielectric photo BCB (12µm) coating and pad opening. Connections of via, metal trace and underpass are shown in Fig.13.

Top metal trace and via have excellent connection because the via and metal trace were formed in the same electrical plating process. The via and M2(underpass) have good connection by the barrier layer Ti shown in the enlarged view of bottom via (Fig.13b). The RF measurement was conducted after wafer process. The 0.72 and 0.81nH inductors within 8 dies at 2.5GHz were measured. Maximum variations of inductances are within 5% in the same structure. Unloaded Q-factors of the measured inductors (0.72 & 0.81nH) are in the range of 30 to 40 at 2.5GHz. Bandpass filter was designed after capacitor and inductor process setup and optimization. Optimized filter was combined inductor with capacitor in the test vehicle as fabricated is shown in Fig.14.

The RF measurement results of the bandpass filters within 5 dies are shown in Fig.15. The filters response is consistent, bandwidth is about 150MHz centered around 2.45GHz with an insertion loss of <2.5dB within the pass-band.

Fig.13 The cross-section of via (a), the enlarged via bottom (b).

Fig.14 The designed filter after fabrication.

Conclusions

In this work, we successfully integrate resistor, capacitor, inductors and filters after solving resistor uniformity issue, optimizing capacitor and inductor scheme. The high Q inductors and bandpass filter were designed and fabricated for WLAN application. Electrical measurement results indicated the fabricated inductors (0.72 & 0.81nH) are able to give an unloaded Q-factor between 30 and 40. The filter’s measured response shows that the designed filter have a bandwidth about 150MHz centered around 2.45GHz with an insertion loss of <2.5dB within the pass-band, also good consistency in the filter is observed from measurement results obtained 5 different dies distributed in the whole wafer.

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References