Integration of Tensile-Strained Ge p-i-n Photodetector on Advanced CMOS Platform

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Abstract - Tensile-strained Ge photodetector is realized on Si-substrate using novel Si/SiGe compliant layer with two-step Ge-process. Monolithic integration of p-i-n detectors with low dark current (0.4 nA), responsivity (190 mA/W) and high speed (>5 GHz) on Ge-CMOS platform is demonstrated, with Ge pMOSFET showing 2X Si hole mobility.

I. INTRODUCTION

Ge-on-Si-substrate photodiodes have recently gained tremendous interest due to their application in low-cost Si-based OEIC for optical communications. Although the 4% lattice mismatch between Ge and Si makes the integration of Ge-devices into Si platform quite challenging, a two-step process has been proposed by Colace et al. accommodating thick flat Ge epilayers on Si [1]. Further improvements by Luan et al. demonstrate threading-dislocation free Ge mesas by combining selective area epitaxy and cyclic thermal annealing [2]. In this paper, high quality Ge grown by selective epitaxial growth on different sized (10-100 μm2) Si window without thermal annealing is presented. Ge-on-Si heterojunction p-i-n diodes fabricated using this method are characterized by AFM, micro-Raman and TEM with flat-surface (rms~0.59 nm), etch pit density ~6x10^10 cm⁻² and tensile-strain of up to 0.67%. The fabricated photodiode shows extended photoresponse covering the L-band with speed > 5 GHz. Using the same Ge-platform, high-speed Ge-CMOS has also been fabricated with high p-drive current of up ~2× universal Si hole mobility.

II. EXPERIMENT

Starting with (100) p-type Si (resistivity ~8-15Ωcm), PECVD oxide ~180nm was deposited, patterned and dry/wet etched to form various area (circular and square shape with area 10-1000 μm²) window for PIN photodetectors and transistors. The bottom of the mesa was then implanted with As/2.2x10¹³ cm⁻²/20 keV and annealed at 1000°C. Ultrathin Si seed (~10nm), Si₈₋₀₂Ge₀₂ (~25nm, 350-400°C) buffer, and (two-step) strain-relaxed Ge were sequentially deposited in a UHVCVD chamber. For the two-step Ge process [1], a low-temperature (400°C) LT-Ge seed (~10nm) was first deposited followed by high temperature HT-Ge (~150nm) deposition at 550-600°C and capped with 3nm tensile strained-Si for CMOS optimization. For compliant buffer development, some wafers incorporate SiGe buffer while other samples have Si/SiGe buffer which has better compliant effects [3]. After standard cleaning process, some wafers were separately deposited with 6nm HfO₂ by PVD sputtering and annealed in O₂ at 700°C. Transistors with gate length of L_g = ~0.5-10 μm were fabricated. All the samples were then implanted with a phosphorous/boron dose of 1x10¹⁵cm⁻² at 5keV at a tilt of 7° and thermally activated at 600°C for 10sec. Finally, ohmic contacts were formed by a metal stack of a thin layer of TaN (25nm) and a 0.75μm Al. Fig. 1 shows the schematic of the p-i-n detector and Ge CMOSFET fabricated on the same Ge platform on separate wafers.

Inset shows the TEM images of the selective epi grown (SEG) Ge on Si/SiGe buffer on Si (160nm). AFM shows a flat Ge surface with rms~0.59 nm for samples with Si/SiGe buffer and 1.06 nm for samples with SiGe buffer.

![Fig. 1 Schematics of fabricated lateral PD and MOSFET on tensile strained Ge-on-Si platform. Inset shows the surface roughness and TEM of SEG Ge on Si/SiGe buffer on Si substrates.](image)

III. RESULTS AND DISCUSSION

(a) Dark Currents in Ge-Photodiode

Current-voltage (I-V) measurement of Ge p+i-n photodiodes on Si/SiGe buffer for circular p-i-n of area 120 μm² shows very low leakage of 0.4 nA at -1V bias under room temperature (300K) as shown in Fig. 2(a) with ideality factor, n ~ 1.19. Dark current under reverse bias, shows relatively flat reverse saturation leakage up to -5V demonstrating good quality Ge with very little generation-recombination even at high field. The low voltage dependency of the reverse bias leakage suggests uniform defect states without dopant permeation into the intrinsic layer [5]. For high temperature operation, low
leakage is an important criterion due to temperature dependence of Ge bandgap and generation-recombination at defect sites. Our devices show good leakage even at high temperature. Dark current increases by a factor of 10 from 30°C to 90°C (3.5 nA at -1V) for a typical 120 μm² lateral Ge p-i-n photodetector. The results are comparable and lower than [5] and well below the 1 μA upper limit for high speed receiver application. Fig. 2(b) shows Arrhenius plot of the dark current $I/pT^{3/2}$ with activation energy of $E_a = 0.32$ eV which corresponds to roughly half of Ge direct bandgap ($\sim 0.66$ eV). The results validate thermal generation and recombination of carriers in the intrinsic Ge layer rather than the underlying Si.

(b) Tensile strained Ge Responsivity

Using two-step Ge deposition at 335°C/700°C, tensile strained (0.25%) Ge has been previously demonstrated [6,7]. In our current work, a compliant Si/SiGe buffer coupled with the two-step Ge at 350°C/600°C has been used. Fig. 3(a) shows the micro-Raman spectroscopy using 514.5nm Ar⁺-laser in the $z(\bar{z},\bar{z})$ backscattering configuration. For samples with Si/SiGe buffer layer, the Raman peak shift by 2.6 cm⁻¹ compared to bulk Ge. The in-plane strain component can be calculated from $\Delta\omega = bE_{\text{z}}$ where $b = -415$ cm⁻¹ using the elastic and strain tensor constant from [8]. From Fig. 3(a), it can be observed that samples with SEG-Ge grown on Si/SiGe buffer layer experience an in-plane tensile strain of 0.63%. Our results for Si/SiGe buffer is significantly higher than [6,7] due to the underlying compliant micro-crystalline Si layer which is expected to have a even lower thermal coefficient of expansion (TCE) [10] compared to Si bulk and SiGe buffer which promote full relaxation of the Ge layer during epi-growth. Samples with SiGe buffer shows 0.12% strain, which matches the results of [6] considering the lower temperature used in our study. As a result of the enhanced tensile strain, the Ge direct bandgap, $E_g$ will be reduced from 0.80eV to 0.76eV, corresponding to $\lambda = 1.62$ μm, resulting in efficient photon detection in the L-band (Fig. 3(b)). Fig. 4 shows the responsivity spectra of the lateral Ge p-i-n photo detector (120 μm²) under normal incidence illumination using laser diode with multi-mode fiber probe at $\lambda = 1.52$ to 1.62 μm. Samples with Si/SiGe buffer show wider photo-response spectral than those with SiGe buffer which could be attributed to the enhanced tensile strain. Fig. 4 inset shows the normalized photo-current (reference to 1520nm) under 0.1 mW laser illumination for samples with Si/SiGe
buffer ($\varepsilon = 0.63\%$) and those with SiGe buffer only ($\varepsilon = 0.12\%$). A wider spectral response for samples with Si/SiGe buffer is observed, well beyond 1580 nm with responsivity of $-190$ mA/W at 1.52 $\mu$m. The responsivity is reasonable considering the thickness of Ge (0.2 $\mu$m) and inherent mismatch between the multi-mode fiber and photo-diode aperture. In comparison, Colace et al. have obtained responsivity of 0.24 A/W at 1.32 $\mu$m [11] for 0.4 $\mu$m thick Ge.

(c) Photodetector speed

The temporal response of several square-shaped 13 $\times$ 13 $\mu$m$^2$ lateral detectors were measured using 1.55 $\mu$m pulsed fiber laser with optical pulse width of 80 fs. Devices were probed with microwave probes and measured with a 15 GHz sampling oscilloscope. DC voltage bias was coupled using a 26 GHz bias tee. Fig. 5 shows the pulsed response and the Fast-Fourier-Transform (FFT) over 1 ns duration for Ge p-i-n with Si/SiGe buffer and SiGe buffer. The 3-dB bandwidth is 5.2 GHz (Si/SiGe buffer) and 1.17 GHz (SiGe buffer) at -1 V and is limited by the electrode spacing of 1 $\mu$m between the n$^+$ and p$^+$ region and lack of de-embedding structure. Enhanced speed in Ge on Si/SiGe buffer correlate with higher tensile strain in the Ge layer and may also be related to better Ge quality as evidenced by lower surface roughness of samples with Si/SiGe buffer.

(d) Integration with Ge-CMOS platform

Using the Ge platform with Si/SiGe buffer, CMOS with HfO$_2$(60 Å)/TaN gate stack has been fabricated. To ensure process compatibility, high thermal processing is avoided, by usage of high-$\kappa$ dielectrics/metal-gate with the thermal processing limited to 700 $^\circ$C, 30s for gate annealing under O$_2$ ambient. Source-drain activation is performed together with the dopant activation for the Ge photo-detector n$^+$ electrode at 600 $^\circ$C, 10 sec. Using this low thermal process flow, Ge CMOSFET had been fabricated with good device performance. Fig 6(a) shows the drive current for p- and n-channel MOSFET fabricated on the same platform shows low dark current of 0.4 nA/ $\mu$m$^2$ detector) at -1V reverse bias with responsivity of 190 mA/W at 1.52 $\mu$m and extended photon detection to 1.62 $\mu$m wavelength. CMOSFET fabricated on this Ge platform shows low dark current of 0.4 nA (leakage < 0.4 mA/cm$^2$ for typical 100 $\mu$m$^2$ detector) at -1V reverse bias with responsivity of 190 mA/W at 1.52 $\mu$m and extended photon detection to 1.62 $\mu$m wavelength. CMOSFET fabricated on the same platform with HfO$_2$/TaN gate stack with low thermal processing flow ($\leq$700$^\circ$C) shows good CMOS performance with hole mobility more than 2× of its bulk-Si counterpart.

IV. CONCLUSION

Using Si/SiGe buffer layer coupled with two step Ge growth process, we are able to increase the tensile strain in Ge layer to 0.63% suitable for photon detection in the L-band. Lateral p-i-n Ge photo-detector fabricated on this Ge platform shows low dark current of 0.4 nA for Ge n-channel MOSFET for $L_g$ = 5 $\mu$m. Mobility measurement using split-CV shows hole mobility in tensile strained Ge (253 cm$^2$/Vs) is more than 2× higher compared to the Si universal mobility (121 cm$^2$/Vs) at 0.2 MV/cm (Fig. 6(b)).

REFERENCES