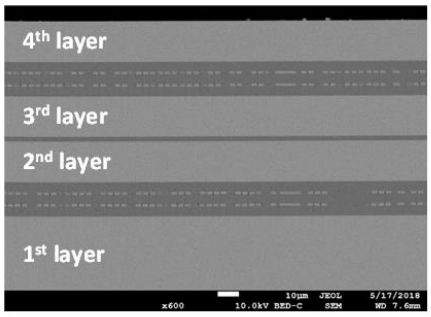
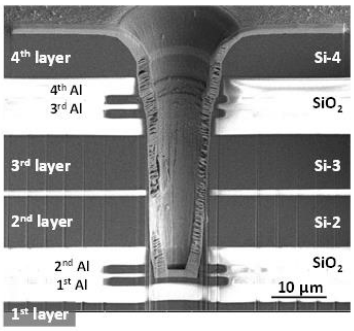
Institute of Microelectronics
IME

3D STACKING PAVES WAY FOR SMALLER, POWER-PACKED COMPUTING CHIPS

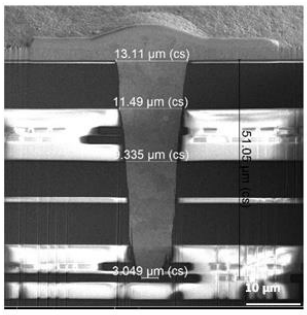
Scientists from the Institute of Microelectronics (IME) at the Agency for Science, Technology and Research (A*STAR) have developed breakthrough technology that can stack up to four layers of wafers, potentially decreasing the cost of production by 50 per cent.



4-layer multiple wafer stacking



Confirmed successful dry etching punching through 4-layer structure



Good Cu filling was confirmed

DEFYING LIMITATIONS TO MOORE'S LAW

Computing performance is struggling to keep up with the relentless drive for higher-performing chips, as performance bottlenecks have emerged with scaling reaching the limit on all fronts. One way to extend Moore's Law is through heterogeneous integration, which can pave the way to future devices with increasing performance levels.

As chips become smaller and more powerful, the wires connecting the growing number of transistors get thinner and more densely packed. The resulting increased resistance and overheating can cause signal delays and limit the central processing units (CPU) clock speed. Other issues include frequency limitations in large-scale integrated circuit (LSI) operations, battery-related power limitations, and cooling problems.

When improving performance in mobile computing and graphic processing systems, one consideration is to ensure that neither the operating frequency nor power consumption is increased. Another consideration is that improving the memory access bandwidth with power consumption efficiency, makes it necessary to have a wide input/output (I/O) memory bus instead of a high-frequency interface. Also, the memory capacity in such systems is becoming more significant as the system performance improves.

3D chip technology helps solve several issues challenging the making of chips with performance increases and processor size reductions. This approach layers one chip or integrated circuit (IC) on another through a process called wafer bonding. The use of the through-silicon vias (TSV) manufacturing approach vertically stacks multiple chip components on each other, creating faster, smaller and lower-power CPUs. TSVs can also enable more efficient heat dissipation and improve power efficiency. With this

approach, multilayer wafer-to-wafer (W2W) stacking for more than two layers with fusion/hybrid bonding technology is critical.

“In the search for cost-effective solutions for 3D integration to implement 3D ICs across a wide range of markets, there is much room for cost reduction from current technology,” said Dr Kawano Masaya, Senior Scientist and project lead at A*STAR’s IME. “Adding a third dimension to an integrated circuit allows Moore’s Law to continue as vertically stacking the layers packs more transistors into the same small footprint,” he added.

INNOVATIVE 3D INTEGRATION

IME has successfully developed a multi-wafer fusion bonding process and a one-step TSV process that can stack up to four layers of wafers. This resulted in an reducing the production cost to 50 per cent.

This significant reduction in cost, coupled with higher volume manufacturing, was made possible by combining Face-to-Face and Back-to-Back wafer bonding with one-step TSV after stacking.

Explained Masaya, the capability to have multilayer W2W stacking for more than two-layers with fusion/hybrid bonding technology is critical for next generation products. This includes a wide variety of applications such as mobile computing, high performance computing and graphic computing require cost-effective 3D integration technology.

“The 3D integration, TSV process and multi-wafer fusion bonding technology breakthroughs will allow device manufacturers to better integrate 3D products with high added value. This development will mean new business opportunities with its low cost 3D-DRAM [3D-dynamic random access memory] and manufacturing, for device manufacturers, equipment suppliers, and material suppliers,” said Masaya.

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About the Institute of Microelectronics (IME)

The Institute of Microelectronics (IME) is a research institute of the Agency for Science, Technology and Research (A*STAR). Positioned to bridge the R&D between academia and industry, IME's mission is to add value to Singapore's semiconductor industry by developing strategic competencies, innovative technologies and intellectual property; enabling enterprises to be technologically competitive; and cultivating a technology talent pool to inject new knowledge to the industry. Its key research areas are in Heterogeneous Integration, System-in-Package, Sensor, Actuators and Microsystems, RF & mmWave, SiC/GaN-on-SiC Power Electronics, and MedTech. For more information on IME, please visit www.ime.a-star.edu.sg.

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