

FACT SHEET

A*STAR'S INSTITUTE OF MICROELECTRONICS PARTNERS EIGHT SEMICONDUCTOR COMPANIES IN CHIP-TO-WAFER HYBRID BONDING CONSORTIUM

11 February 2021

A*STAR's Institute of Microelectronics (IME) has partnered leading semiconductor companies to develop Chip-to-Wafer (C2W) Hybrid Bonding for high density 2.5D and 3D integrated circuit (IC) integration. The newly formed pre-competitive C2W Hybrid Bonding Consortium with international and local industry supply chain companies will leverage IME's expertise in 2.5D and 3D IC integration and bonding technologies for the development of C2W hybrid bonding process and demonstration of 4 chips stacking with $\leq 10\mu\text{m}$ pitch interconnections. Refer to **ANNEX A** for the full list of consortium members.

The C2W Hybrid Bonding Consortium led by IME consists of leading global industrial players and an SME in Singapore ranging from device manufacturers to equipment and material suppliers. Device manufacturers contribute to the design, process and reliability requirements, whereas the equipment suppliers contribute by bringing new state-of-the-art tools and capabilities plus developing and modifying the hardware dedicated for hybrid bonding, and module process development. Material suppliers would bring along new dielectric materials for hybrid bonding as well as temporary adhesives for thin wafer handling. Local SME, Capcon Singapore brings to the consortium their strong expertise in making Flip-Chip Bonder; primarily high precision high productivity Die Bonder and Flip-Chip Bonder, Chip-on-Wafer Bonder and Package-on-Package Bonder capabilities. As a member of the consortium, Capcon is able to accelerate their research and development and shorten their development cycle in the area of chip-to-wafer hybrid bonding. Together with the consortium members, IME will lead the development and the process integration to achieve high yield multi-stack C2W hybrid bonding.

The need for higher speeds and larger memory capacities continues to grow, due to the huge amounts of data storage and data processing required for data centres and high performance computing (HPC) applications. In addition, system-on-chip (SoC) is moving towards "chiplets" with high-density 2.5D/3D integration. Mix-and-match functional chiplets are able to reduce design cost and time by reusing existing IPs and dies, while conventional 2D scaling does not reduce chip cost anymore. Based on the strong demand for high-density 3D stacked memory and 2.5D/3D heterogeneous integration, fine pitch inter-chip connection is of great interest to the semiconductor industry. C2W stacking using hybrid bonding is key to achieving these demands as well as fine pitch interconnections and small form factors.

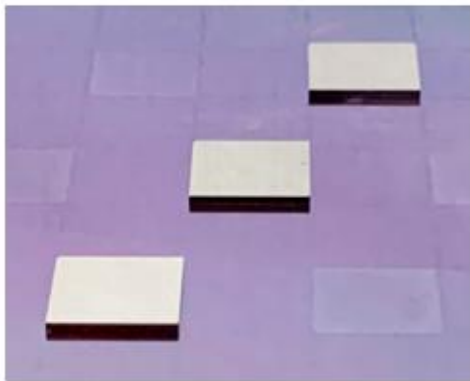


Figure 1. C2W Hybrid Bonding

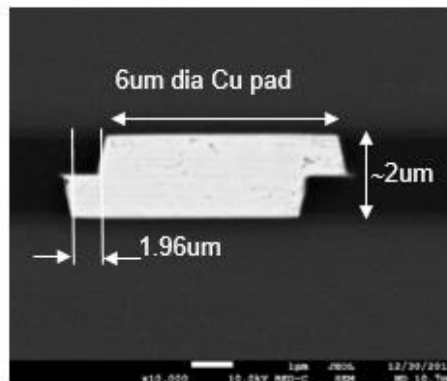


Figure 2. Cross section of C2W Hybrid Bonding

2.5D/3D stacking today uses copper-pillar based micro-bumps for inter-die vertical interconnections using chip-to-chip or chip-to-wafer bonding. Cu-pillar micro-bumps have a limitation of $\sim 20\mu\text{m}$ in the smallest pitch that can be achieved. Below $20\mu\text{m}$, solder bridging is a roadblock for further pitch reduction. Increasingly, industry is moving to bump-less interconnections using Copper-Copper (Cu-Cu) hybrid bonding to achieve ultra-fine interconnections at $\leq 10\mu\text{m}$ pitch. In this technique, the dies/wafers are prepared with excellent flatness (dishing $< 10\text{nm}$, roughness $< 0.5\text{nm}$) and with high degree of surface cleanliness to achieve high quality bonding between copper-pads of the die/wafer being bonded and oxide areas separating the copper-pads. As such, achieving wafer flatness and cleaning is key to achieve high yielding hybrid bonding technology.

The C2W Hybrid Bonding Consortium aims to bridge this interconnect gap through development of various processes required for hybrid bonding technology that could support $\leq 10\mu\text{m}$ pitch. The consortium plans to also develop a multi-chip C2W stacking up to 4 chips for applications such as DRAM, NVM, HPC which require cost-effective 3D integration technology for next generation products of the above applications.

Breakthroughs by C2W hybrid bonding technology will allow device manufacturers to better integrate 2.5D/3D products with high added value, such as memory stack, logic and memory system-in-package, and chiplets. Such technologies could open up new business opportunities for not only device manufacturers, but also equipment suppliers and material suppliers related to hybrid bonding and process integration technologies.



For media queries, please contact:

Ms Lydia Sum
Assistant Head, Corporate Communications, A*STAR
Tel: +65 9825 3600
Email: sumcll@hq.a-star.edu.sg

About the Institute of Microelectronics (IME)

The Institute of Microelectronics (IME) is a research institute of the Agency for Science, Technology and Research (A*STAR). Positioned to bridge the R&D between academia and industry, IME's mission is to add value to Singapore's semiconductor industry by developing strategic competencies, innovative technologies and intellectual property; enabling enterprises to be technologically competitive; and cultivating a technology talent pool to inject new knowledge to the industry. Its key research areas are in Heterogeneous Integration, System-in-Package, Sensor, Actuators and Microsystems, RF & mmWave, SiC/GaN-on-SiC Power Electronics, and MedTech.

For more information on IME, please visit www.ime.a-star.edu.sg.

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- A*STAR's Institute of Microelectronics
- ASM Pacific (Hong Kong) Ltd
- Capcon Singapore Pte Ltd
- HD MicroSystems, Ltd
- ONTOS Equipment Systems, Corporation
- Panasonic Smart Factory Solutions Co., Ltd.
- SEKISUI CHEMICAL CO., LTD.
- Toray Industries, Inc.
- Yamaha Robotics Holdings Co., Ltd.