Institute of Microelectronics
A*STAR

FABRICATION & PACKAGING SERVICES

Our Technology Your Business

Wafer Fabrication Services

Institute of Microelectronics (IME) Fab offers a broad range of services to our customers to meet the research and development (R&D) needs for semiconductor and related industries.

IME's Fab is located in-house and provides R&D services on micro-electro-mechanical systems (MEMS), microelectronics nanotechnology and bioelectronics applications. IME offers advanced lithography patterning services for 45nm half pitch features in small volume production in Class-10 clean room. Our Immersion Scanner is supported with metrology and defect tools and successfully demonstrated flat optics device functionality on 12" silicon and glass wafers.

Lithography
- i-line Steppers (<2um CD)
-ArF Immersion scanner (<45nm CD)

Physical Vapor Deposition
- Cu Seed
- Al/ AlO_2
- Ti / TiN
- HfO_2 / HfN

Chemical Vapor Deposition
- TEOS
- Silicon-Nitride

Electroplating (ECP)
- Cu RDL, UBM
- TSV Cu Pillar

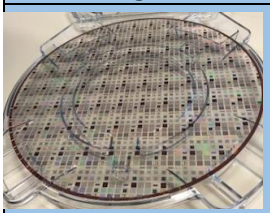
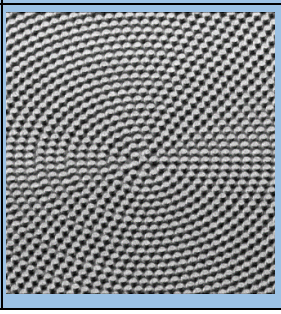
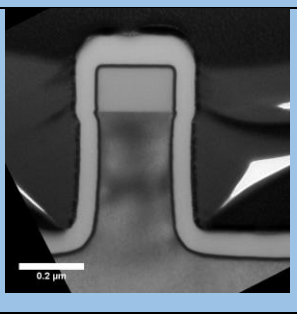
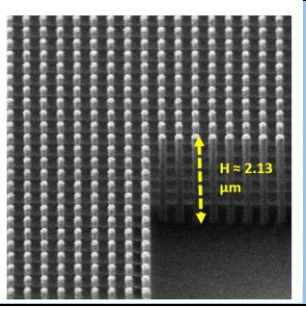
Bonding
- Temporary/permanent
- Fusion
- Polymer
- Hybrid
- Metal

Metrology
- Macro & Micro Defect Review
- Defect Review SEM
- Sidewall Roughness
- Surface Morphology
- Film Stress/ Warpage
- Film Thickness measurements

Furnace
- Anneal
- Polymide , Dielectric Cure

Etch
- Descum
- Silicon
- Oxide
- Silicon-Nitride

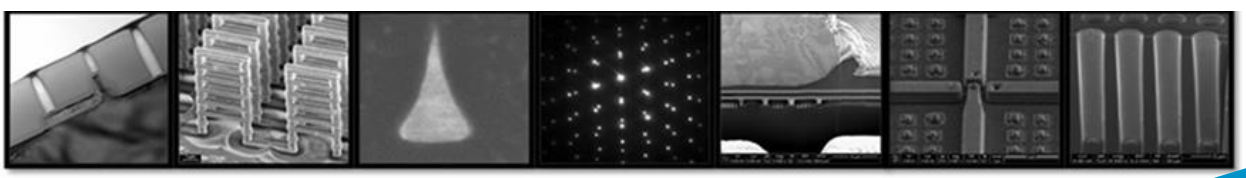
Customized Solutions
- Specialty CVD/ PVD depositions
- New materials evaluations
- Deep machines learning applications

12in Glass Wafer Patterning	Focal lens	ALD	High Aspect Ratio Etching>10
			

Material Defects & Reliability Analysis Services

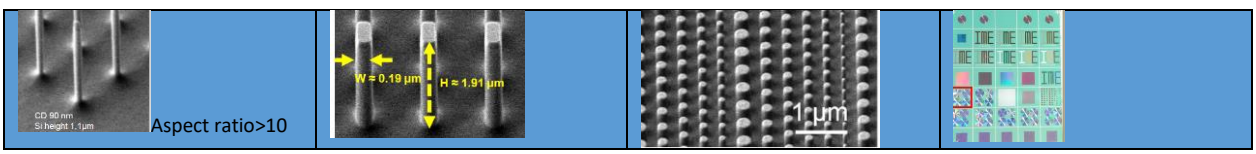
Material defects and reliability analysis (MDRA) are essential for microelectronics research, development and manufacturing. Our MDRA lab has the capabilities and cutting edge facilities to conduct world class research and development in semiconductor technology. We provide materials and process characterization, failure analysis and reliability test to support our industry partners in wafer fabrication, packaging, assembly and test.

MDRA Tool Capabilities	
Tools	**Tool capability**
12" Probe station	• Automation IV, CV measurement on 12" wafers
FEI Double beam FIB	• Up to 65nA Ga^+ beam current under 30KV • High resolution SEM/STEM images (<0.1nm) • TEM sample preparation avaliable inside the machine
FE- SEM	• High resolution SEM image with EBSD and EDX analysis (<0.1nm) • Probe in SEM to measure IV curve
Ar Ion Milling/Polisher	• Sample preparation for SEM, FIB and optical microscope analysis
CSAM Sonix	• Transducers from 15 KHz to 230MHz for C-Scan/T-Scan analysis • 12" warp wafer compensation
Thermal Shock Chamber	• Test standard JESD22-A104 • Temperature range (-70°C to 300°C)
ESD tester	• Machine mode/Human body mode
High temperature storage chamber	• Test standard JESD22-A103 • Temperature storage up to 300°C
Thermal Shock (liquid to liquid)	• Test standard JESD22-A106 • Temperature range (-65°C to 200°C)
Thermal Humidity Chamber	• Test standard JESD22-A101 • Temperature stress: 85 °C, relative humility stress: 85 %
FEI TEM (CM200)	• 200KV transmission electron beam analysis (resolution <0.14nm) • EDX/EELS analysis
3D X-Ray	• None destructive 3D X-Ray imaging • High spatial resolution to 500nm
XB550	• FIB-SEM for 3D Analysis (resolution <0.1nm)



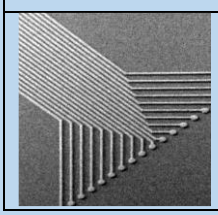
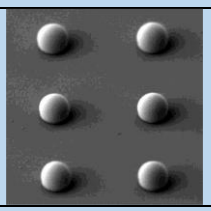
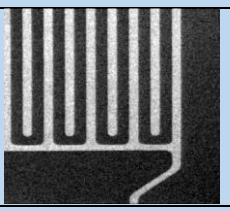
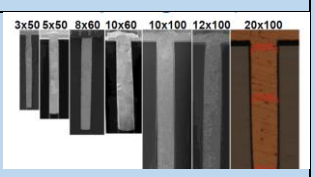
FAB Capabilities

12inch FAB Capabilities	
Module	**Unit Process capabilities**
Photo Lithography	• TSV Steppers with <2um patterning capability
	• Resist/Dielectric Polymer Coating
	• Fine Lithography with Immersion Scanner for <45nm patterning capability
Thin Films	• PVD Seed Layer Deposition (Ti/Ta/Cu) (2x12/3x50/5x50/10x100/20x100um with max aspect ratio of 10~15)
	• TSV Cu filling (2x12/3x50/5x50/10x100/20x100um with max aspect ratio of 15) • Damascene Cu (CD>=1um, max aspect ratio of 2)
	• Cu RDL (Line/Space: 1/1um), Cu Pillar (CD >10um, max aspect ratio of 2)
	• UBM Cu/Ni/SnAg (CD >10um, max aspect ratio of 2)
Spin Coat	• Coating of Under fill/Flux/Polymers with & w/o Dicing Ring
Dry etch	• Si etch for 5X50um & 10X100um TSV • Si nano-structures etch of aspect ratio >10 with <60nm CD • Metals etch with In-Situ PR Removal
Clean	• Ti/Cu etching
	• Low temperature Photo Resist Stripping capability with Al/Cu compatible • Post-RIE polymer removal • Wafer front-side/backside cleaning • Descum/Ex-Situ PR Removal
CMP	• Cu & Barrier Layer CMP
Bonding	• Anodic, Solder, Polymer, Temporary & Permanent bonding
	• Post Debond Cleaning
12" In-Line Metrology	• Dielectric & PR Film thickness measurement with Spectroscopic Ellipsometry (SE) or Broadband Dual-Beam Spectrophotometry
	• Metal Sheet resistance measurement
	• Optical CD Measurement (<0.1nm accuracy)
	• CDSEM measurement (<0.35nm accuracy)
	• Overlay measurement (<0.1nm accuracy)
	• Wafer bevel and backside defect inspection (<0.5um)
	• Wafer macro and micro defect inspection and review
	• Unpattern wafer defect inspection (<26nm)
	• Pattern defect inspection (<30nm)
	• Defect SEM review with EDX and ADC (auto defect classification)
	• Cu profiler step height measurement for step height <500um
	• Film stress or warpage 5 layer film parameter measurement
	• Side Wall roughness 3D AFM measurement with <2A RMS noise level
	• Surface morphology 2D AFM measurement with lateral accuracy



FAB Capabilities

8inch FAB Capabilities	
Module	**Unit Process capabilities**
Photo Lithography	• I-line Resist Coating & Patterning with 0.5um resolution and Front to Back Alignment
Diffusion	• Cu Annealing up to 600°C in N2 / 450°C in foaming gas
	• Passivation Curing up to 600°C in N2
Thin Films	• Specialty Metals - Mo/ AlN/ Al2O3/ HfO2 /ScAlN
	• Dielectric films - USG, SiN up to 400°C
	• Cu RDL (Line/Space: 1/1um), Cu Pillar (CD >10um, max aspect ratio 2)
	• TSV Cu filling (10x40 and 20x100 with max aspect ratio up to 15)
	• Damascene Cu (CD>=1um, max aspect ratio 2)
Spin Coat	• Polyimides, Organic Polymers
	• Anti-Stiction Coating
CMP	• Cu CMP and Barrier Layer CMP
Release Process	• Oxide structures release capability for silicon depth up to 200um by XeF2
	• Silicon structures release capability for sacrificial oxide depth up to 200um by HF Vapor
Bonding	• Anodic, Solder, Polymer, Temporary & Permanent bonding (Low & High Force)
	• Post Debond Cleaning
In-line Metrology	• Infrared film thickness measurement with accuracy of +/-0.5mm
	• Sheet resistance measurement in the range of 5ohms to 5MOhms.

Electroplating Cu RDL (>2um line/space, 8/12inch)	Electroplating bump (Cu/Ni/SnAg, >20um, 8/12inch)	Cu Damascene (>2um line/space, 8/12 inch)	Electroplating TSV (3-20um Via, 8/12 inch)
			

Packaging Design & Fabrication Services

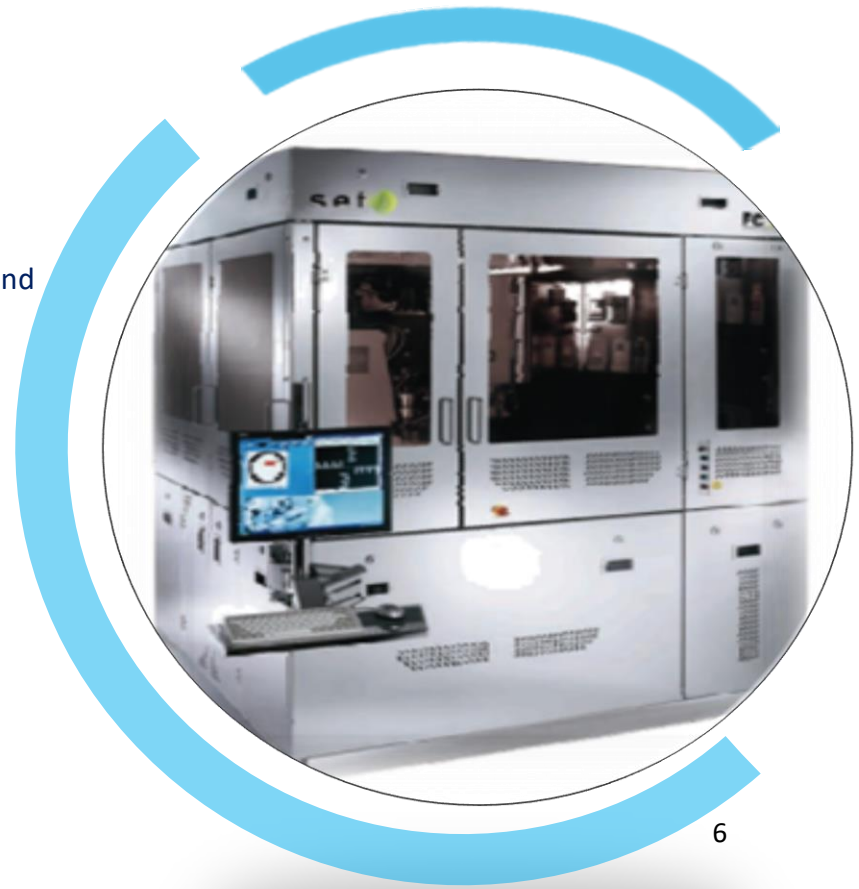
IME offers a wide range of advanced packaging technology solutions to address the above industry needs. Our platforms include 2.5D through-silicon interposer, 3D TSV, fan-out wafer level packaging, MEMS wafer level chip-scale packaging, fine-pitch Cu pillar, chip-on-wafer (direct Cu-to-Cu) bonding, electronic-photonic integration, as well as thermal solutions.

Services

- Advanced packaging turnkey solutions for industry applications
- Thermo-mechanical, electrical, and thermal modeling and simulations to provide design guidelines
- TSV and through-silicon interposer (TSI) fabrication for 2.5D/3D IC packaging
- TSV fabrication and assembly for image sensor applications
- MEMS wafer level chip-scale packaging
- FOWLP demonstration for new products
- FOWLP re-constructed wafers for equipment and material evaluations

Facilities

- 3000m^2 of cleanrooms
- 200mm and 300mm TSV engineering line
- 300mm FOWLP development line
- Assembly and packaging lab
- Package/board level reliability testing and failure analysis facilities



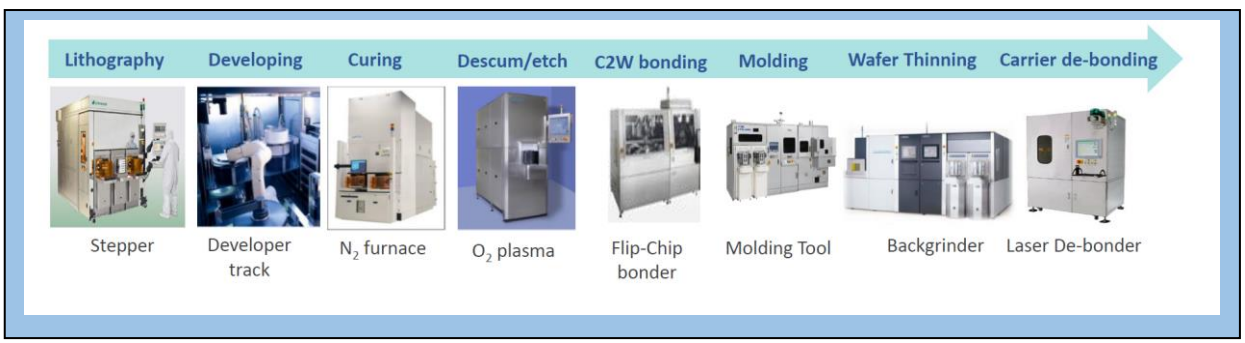
IME's Multi-Chip 12" FOWLP Development Line

IME has state-of-the-art 300mm advanced wafer level packaging engineering line which can support various advanced wafer level packaging technologies development used in mobile, AI, Data Centre and IoT applications.

At IME, we offer end-to-end solutions in FOWLP & 2.5D/3D packaging and shorten the development cycle time for new applications. We also offer services in the area of wafer level fine pitch RDL of 2um/2um LW/LS, C4 solder bumping & Cu pillar micro bumping up to 20um pitch, temporary bonding & de-bonding, TSV fabrication etc.

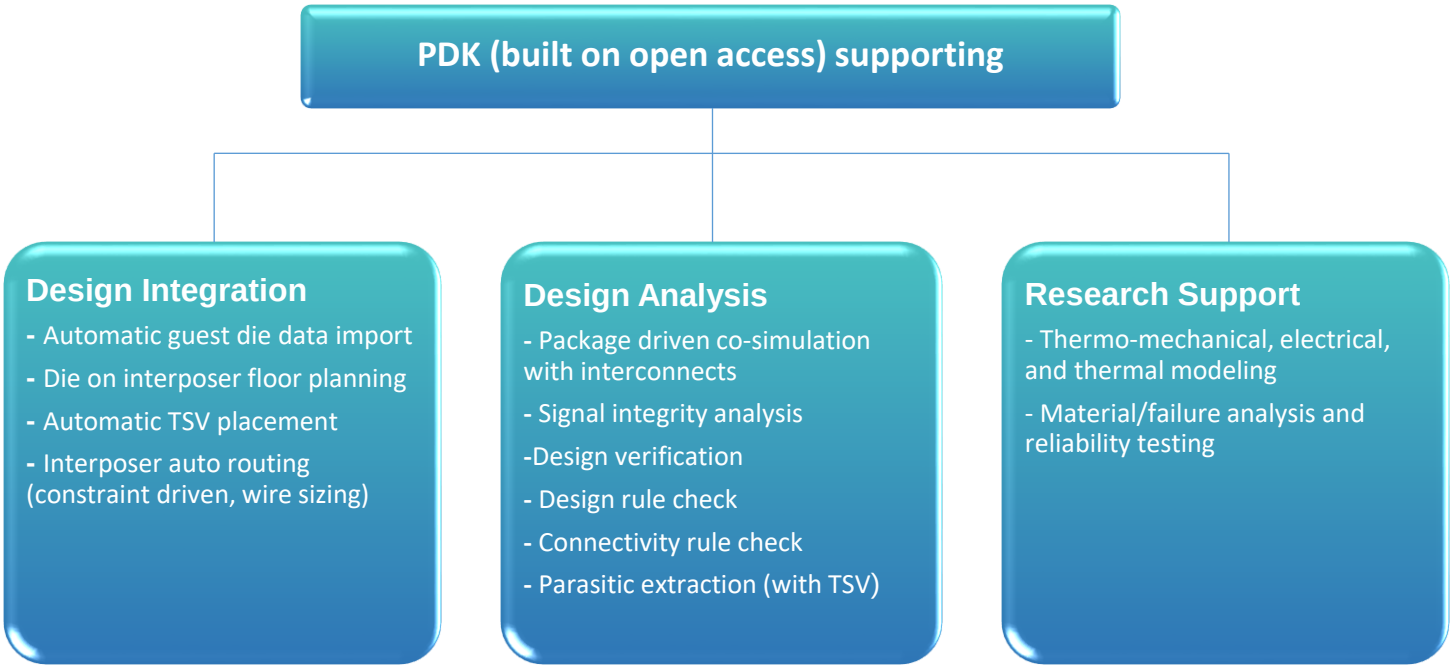
IME's full fledge of development line comprises state-of-the-art tools including

- PVD chamber for seed layer deposition
- PR track for coating and developing
- Stepper for lithography
- Plating (Cu, Ni, Au, SnAg),
- Wet bench for PR stripping
- Spray etcher for seed etching
- N_2 furnace for curing
- O_2 plasma for descum/etch
- Flip-chip bonder for chip-to-wafer bonding
- Molding tool for wafer level compression
- Warpage adjuster for molding tape de-bonding and warpage adjustment
- Backgrinder for wafer thinning
- Laser de-bonder for carrier de-bonding
- Solder jetter for solder ball attach
- Wafer dicer for wafer sawing



One-Stop Solution

IME provides a one-stop solution from system concept, design integration, fabrication and testing to final packaging.



Your Ideal Partner for Realizing Advanced Packaging Solution

- Accurate Package Process Design Kit for realizing TSI and FOWLP system designs
- Reference design implementation flow using multiple off-the-shelf sign-off quality EDA tools
- Physical implementation automation to reduce design and analysis turn-around time

IME is committed to protect customer's IP and confidentiality and provide the best supports to customers.

Contact Detail:

2 Fusionopolis Way, #08-02 Innovis, Singapore 138634
(65) 6501 1800
www.a-star.edu.sg/ime
ID@ime.a-star.edu.sg / FabServices@ime.a-star.edu.sg

An ISO 9001 and ISO 13485 Certified Organisation