Title: Methodologies for material characterization, modelling, and non-destructive fault localization to enhance quality and reliability of 2.5D IC packages

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2.5D integrated circuit (2.5D IC) packaging technologies have seen significant commercial success in recent years. Due to the increasing I/O count, I/O density and large package size from high-performance, and networking applications for 2.5D ICs, ensuring quality and long-term reliability of 2.5 IC packages continues to be a focus in terms of manufacturing operations. To address these concerns, A*STAR's IME and Xilinx have successfully demonstrated novel and improved methodologies for: (a) material testing and mechanical reliability modelling and (b) non-destructive fault localization for 2.5D IC packages.

Material testing and mechanical reliability modelling

Thanks to the excellent electrical, chemical, and mechanical properties, polymeric materials have been widely applied in large-volume manufacturing in the advanced packaging. In Yole's report, the polymeric materials market revenue is predicted to double over the next five years. Polymeric materials can be found in many integration process steps: RDL, bump/UBM, TSV, and assembly levels, as well as at the bonding interface. They have shown increasingly importance in manufacturability, performance, and reliability in advanced electronics applications because the package materials strongly affect the product performance and reliability. Despite the superior properties, polymeric materials usually degrade under thermal ageing conditions. Such material degradation will adversely affect the package reliability performance. However, in the past, the material characterization was mostly done under time zero conditions, i.e. without thermal ageing. As a result, it is not possible to predict the product failure caused by material degradation under thermal ageing conditions. This imposes great challenges for the product reliability performance assessment.

With the aim of providing better understanding on the thermal ageing induced polymeric material degradation, new material characterization methodologies and modelling approach are developed. This is important as Xilinx's products serve markets with a broad range of quality and reliability requirements and as such, must qualify their products to ensure that the products have sufficient reliability margin in the most stringent application conditions with the appropriate level of quality. The developed material characterisation methodologies are able to capture the material thermal-mechanical properties shifts under thermal ageing conditions for modulus, Coefficient of Thermal Expansion (CTE), and the volume shrinkage after high temperature storage (HTS) testing. Meanwhile, in order to predict the thermal ageing induced package failure as early as in the design stage, a novel numerical Finite Element Analysis (FEA) approach using

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swell-strain model is developed. By incorporating the measurement results from material characterization test into the modelling, the swell-strain model can successfully predict the stress caused by the material shrinkage due to both thermal shrinkage and under thermal ageing shrinkage at the same time.

With a strong culture of continuous improvement, Xilinx ensures that the products shipped are always compliant to the demanding quality and reliability needs of the markets they serve. The developed material characterization and modelling methodologies have thus been implemented into the reliability assessment study on a 2.5D IC package with TSV interposer as sketched in Fig.1. The study focused on the underfill material as it is the key material to bridge die, interposer and substrate, and thus reduces the solder bump stress. Its performance during the whole life cycle is important to maintain the overall package reliability. Firstly, material characterization tests are performed on bulk underfill samples. The underfill material property shifts under different thermal ageing conditions are measured and are compared with the results for time zero samples. It is found that the thermal ageing effect on underfill CTE is not significant as the underfill samples show only slightly lower CTE after thermal ageing. For modulus, thermal ageing reduces underfill storage modulus below Tg while increases above Tg. Therefore, thermal ageing makes underfill stiffer and less deformable at high temperature (>Tg). This may lead to high stress within underfill. The measured underfill volume shrinkage is also found to increase with longer thermal ageing duration. Such increase may cause higher stress inside underfill as well as at the interfaces with surrounding materials. Hence, the impact of such ageing effect needs to be well-understood and addressed.

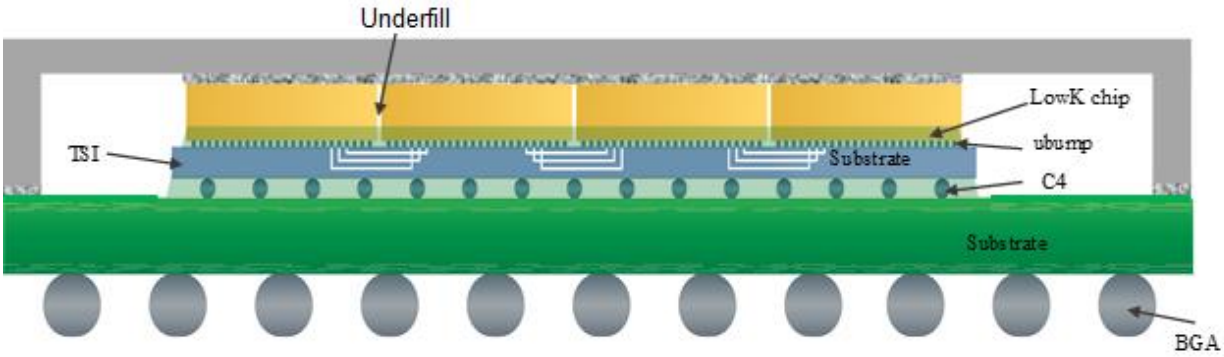

Figure 1. Schematic of 2.5D IC package with TSV interposer.

The thermal ageing induced underfill material degradation measurement results are subsequently taken into FEA simulations. As shown in Fig.2(a) &2(b), high stresses are predicted at the top and bottom interfaces of underfill in the gaps between chips and near TSI die corner. In Fig.2(c), the maximum underfill shear stresses predicted by the

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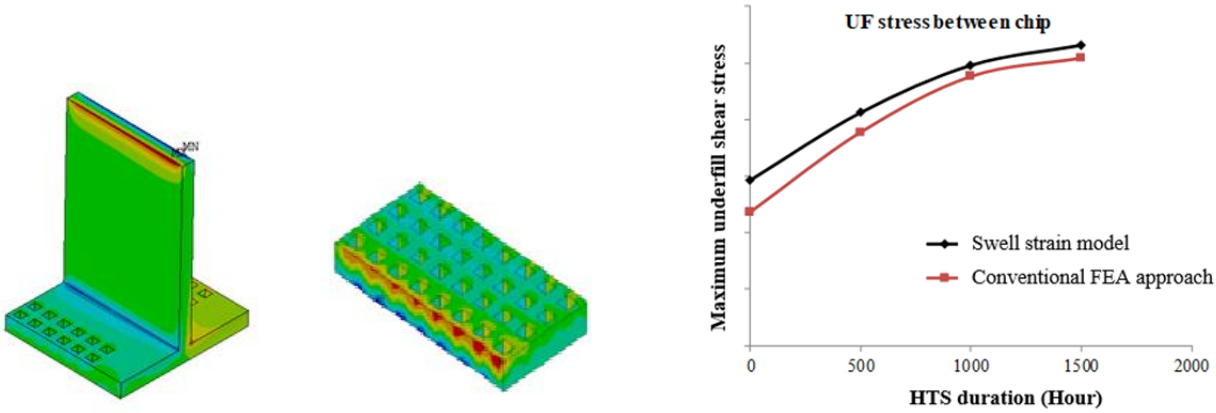
newly developed swell strain model are compared with those predicted by the conventional FEA approach. For both modelling approaches, underfill stress increases with the increasing thermal ageing duration.



Stress of underfill (a) between 2 chips (b) Near TSI die corner (C) Effect of HTS thermal aging duration

Figure 2. FEA modelling results.

This collaboration demonstrated that the material characterization and modelling methodologies developed in this study are able to accurately predict the stress and potential risk for 2.5D IC package. With the well characterized material properties and established modelling methodology, the overall package reliability is predictable under different customer applications, and the potential risk is under well-control.

Non-destructive fault localization for 2.5D IC packages

Accurately identifying the exact location of a defect is critical to improving product quality especially for multi-chip 2.5D IC packages. Investigating yield-loss and reliability mechanisms of such packages is made particularly challenging by the multitude of possible failure locations such as in TSV, micro-bumps, underfill, solder ball joints, and RDL layers. Without accurate fault localization, failure analysis is both cumbersome and often dependent on a best-guess approach which tends to be time-consuming and relatively expensive to be implemented. Current electrical and physical failure analysis tools do not have sufficient capability and/or resolution to accurately localize the failure location in 2.5D IC packages to the desired accuracy. To address the need for a rapid, cost-effective technique, we demonstrate a methodology to localize interconnection failures in 2.5D IC packages in a non-destructive manner with an accuracy of less than 10μm. The faults are detected by an automated test equipment, and then localized by applying terahertz pulse through the interconnects and subsequently, confirmed by employing a non-destructive 3-D x-ray microscopy imaging.

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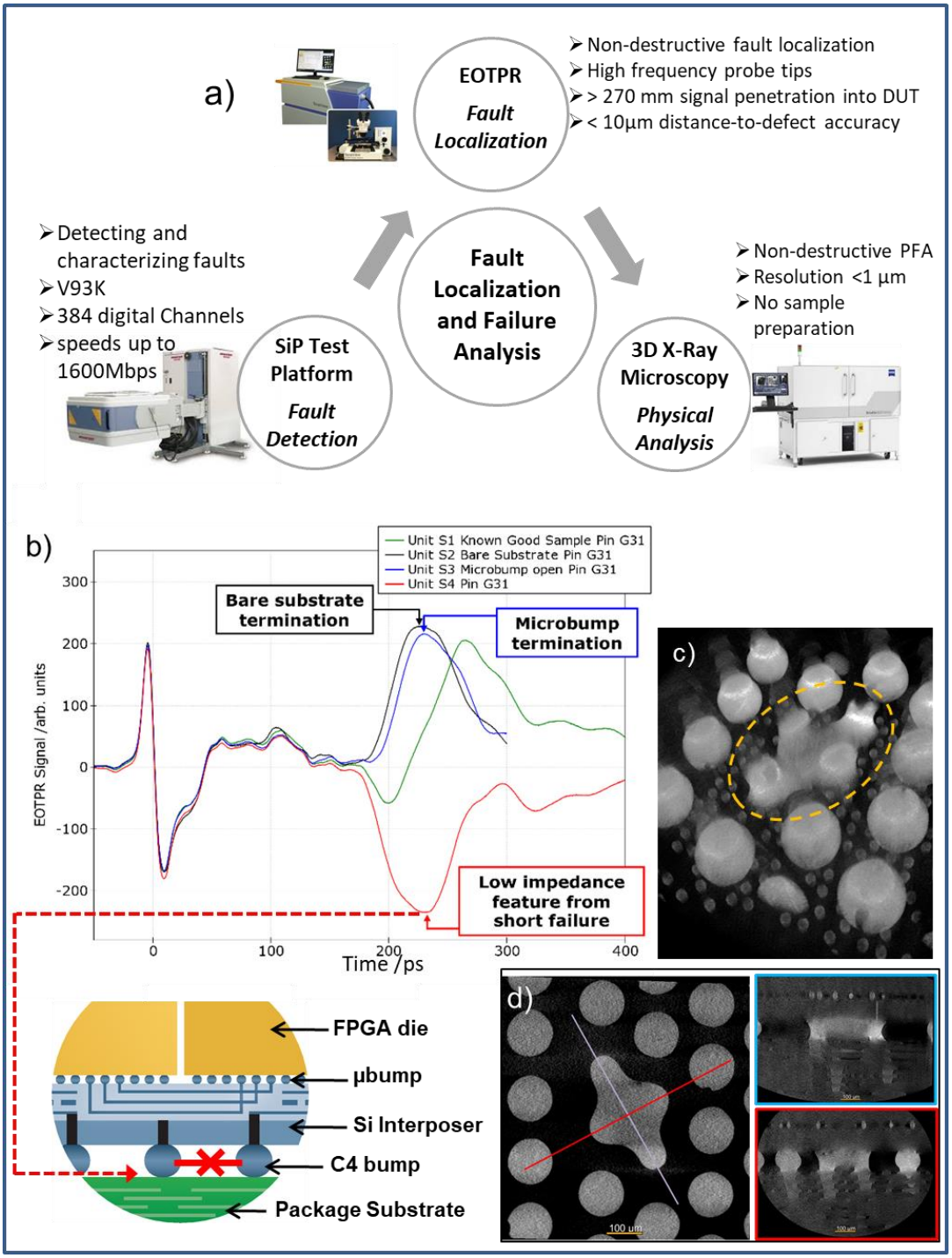

Figure 3. a) Methodology of fault localization. b) A short failure localized by sending terahertz pulse along interconnects of 2.5D package. X-ray images of localized defect c) 3-D image of shorted bumps d) 2D images of the failure extracted from 3D volume data showing the cross-section from the different orientations.

A Multi-channel SoC Automatic Test Equipment (ATE), which is an established tool to detect defects in a package is used to identify the faulty pin. However, ATE results

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cannot define the correct location of the failure in a package. Therefore, an improved technique called EOTPR is engaged to localize the failure. It is capable of localizing shorts, leakages, and open failures in different device architectures rapidly and non-destructively with good localization accuracy. High-frequency electrical pulses are injected into the device under test (DUT) through a probe, which is contacted to the DUT solder ball using a probe station. A photoconductive switch records the reflection of the launched signal caused by structures within the device and faults as a voltage-time waveform. By making use of this time-based data, faults inside advanced packages are localized with minimal references to the internal structure. To assist and evaluate the defect localization, a model is created which employs a one-dimensional lump circuit model to quickly simulate the measured data. The simulation enables equivalent circuits to be defined as elements in a sequence that may include RLC impedances and transmission lines with radiative transmission losses. The process of creating the model can be completed in not more than 30 minutes and the optimized model can be saved for subsequent usage. The complete defect localization procedure typically takes less than 5 minutes while importing a waveform of a failed sample into a pre-optimized model. Post defect localization, the faults are non-destructively visualized and confirmed by utilizing a 3-D x-ray microscopy (XRM) imaging method. XRM can non-destructively pass through advanced IC packages with multiple stacks and image internal structures with a high resolution of <1 μm without damaging the sample. Besides the nondestructive capability of this technique, it does not need any time-consuming sample preparation steps. As it offers images of the internal structures in 3D, it facilitates a detailed study of failures by providing limitless cross-sectioning from all preferred angles virtually. Here, good resolutions are accomplished even for large samples by utilizing a two-stage technique – geometric and optical magnifications facilitated by multiple objectives. In comparison, conventional Micro-CT employs geometric magnification and as a result, the resolution diminishes intensely while processing large samples.

Fault localization methodology for a through-Si-Interposer-based 2.5D ICs package comprising of dies assembled on to the silicon interposer which is then assembled on the organic substrate is described in Fig. 3. The fault was found to be a short defect implied by a distinct low impedance feature from the EOTPR experiment (Fig. 3b) and the location of the defect was identified to be at C4 bump near to the substrate surface. Fig. 3c and 3d show the 3D and extracted 2D images of the short between four C4 bumps. The potential root cause for such defect could be due to the bridging of bumps induced by package warpage during reflow or particulate issue. The developed methodology can be successfully applied to carry out rapid non-destructive failure analysis of 2.5D IC packages by accurately localizing the defects which are internal to the package.

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