List of PhD Projects Offered in Institute of Microelectronics (IME)

Supervisor	Project Title	Description
Dr. Chui King Jien	2.5D/3D Integration of Superconducting Qubits for Quantum Computing	1) Investigation of superconducting materials and fabrication of Superconducting interconnects, Qubits devices for performance and scalability to enable Quantum Computing. Areas of research can include evaluation of materials at cryogenic temperatures, design and fabrication of Josephson Junction Qubit devices, state-of-the-art 2.5D and 3D integration and advance packaging of ASIC chips with Qubit devices capable of operation down to sub-K cryogenic temperatures. 2) RSFQ Circuitry design and fabrication. RSFQ circuitry provides an alternative to CMOS logic circuit for qubit device control. Areas of research include design of RSFQ circuits for control of qubits, design and fabrication of qubit devices, and using 300mm state-of-the-art packaging line for material evaluation and fabrication of the RSFQ circuits.
Dr. Chui King Jien	Design, Fabrication and Characterization of Silicon Carbide (SiC) Interposer	Silicon Carbide (SiC) demonstrates better thermal conductivity, and higher electrical resistivity (or reduced losses) in comparison to Silicon. As such, SiC-interposer is an ideal choice for enhanced thermal management in very high power and high frequency applications. Student will evaluate SiC of different crystalline phase, followed by design, fabrication and characterization of a high performance through SiC Interposer packaging platform.
Dr. Chui King Jien	Fabrication and Characterization of Novel High Density MIM Trench Capacitors	High-density capacitors are required in circuitry involving RF decoupling, Integrated Voltage Regulator (IVR), and high performance computing. Novel high density MIM trench capacitor designs will be explored for system package integration for improved performance, reduced form-factor and cost reduction. This includes investigation of capacitor dielectric material, integration/packaging schemes and electrical/reliability characterization.
Dr. Chui King Jien	Fabrication, Characterization and Heterogeneous Integration of HEMT Devices	Fabrication and characterization of HEMT devices (at NUS). 2.5D/3D integration of HEMT devices with logic and other chips.

		In addition to the fabrication of HEMT devices (e,g, InGaAs, GaAs, GaN), candidate will be exploring processes for the 2.5D/3D integration of HEMT devices with CMOS logic chips.
Dr. Lee En-Yuan Joshua	Biologically Interfaced Acoustofluidic Microelectromechanical Systems for Multiplexed Single-Particle Mass Spectrometry	This project will leverage capabilities developed in the Nanosystems on the Edge program. The work seeks to leverage and extend the capabilities of microelectronics to create new generation advanced chips for probing biological phenomena at the large scales provided by microelectronics. The student will be working to create advanced structures to interact with particles suspended in fluids for different functions including dexterous position control of particles/cells as well as characterizing single-particle mass. Such advanced tools have applications for both fundamental studies as well as food/nutrient processing that include statistical mapping of a large number of particles/cells within a short time period. The outcomes and capabilities arising from this project will serve to advance the future of microelectronics that includes penetrating important emerging applications such as biologics, creating a powerful platform for truly interdisciplinary work.
Dr. Navab Singh	Ultrahigh Voltage Power MOSFETS on Engineered Silicon Carbide Substrates	After a long gestation period, silicon carbide (SiC) devices are in high commercial attraction for highly efficient power switching and conversion applications in various sectors. Charge balance principles, first developed for Si power devices, are being explored with SiC to create super-junction (SJ) MOSFETs to handle ultrahigh voltage without increasing specific on resistance (Ron,sp) of the device. However, SJ implementation require many additional masking and implantation steps which in conjunction with high cost of silicon carbide wafer makes manufacturing of SJ-MOSFET in SiC too costly for mass implementation. In this project student will explore different ways to reduce manufacturing cost of SiC SJ-MOSFETS without compromising performance, yield and reliability of the device. Not limited to, but one of the options could be the use of a trench based SJ utilizing deep etch, conformal sidewall doping, selective epitaxial deposition

		and planarization. To reduce the cost further, trench-fill method can be realized on engineered substrate where a thin 4H-SiC seed layer may be bonded to a poly-SiC substrate before epitaxial growth of SiC for creating active device, field limiting rings (FLRs), and drift layer. Student will be fully responsible for the following: 1. Detailed literature review of SiC power devices to benchmark the performance and challenges to define the problem. 2. Designing of novel SJ device architecture including field termination rings and developing process flow and process conditions using TCAD simulations. 3. Hands-on implementation of the designs and process flow to fabricate the device on 6”/8” engineered as well as conventional SiC wafers. 4. Characterize and analyze the performance and reliability of the fabricated devices and then benchmark with literature. 5. Propose and implement solutions for any loss of performance due to poor thermal behavior of the engineered substrate. 6. Repeat the design and experiment with updated TCAD model parameter until results are satisfactory. 7. Develop analytical models to predict device characteristics. 8. Provide future development directions.
Dr. Prakash Pitchappa	Reconfigurable Intelligent Surfaces (RIS) for 6G Communications	6G communication is expected to use terahertz (THz) as carrier waves. However, the higher frequency of THz waves suffers from increased propagation loss. To counteract this fundamental loss, beam-forming solutions are adopted. But, this leads to line of sight links and needs dynamic beam steering solutions for seamless connectivity to mobile users. Current THz beam steering solutions such as massive MIMO or phased array antennas suffer from high power consumption and high cost. More importantly, the cost, size, weight, and power consumption (C-SWaP) of these approaches scale up drastically with the number of antenna elements. Hence, alternative solutions with low C-SWaP is essential for widespread adoption of 6G links, which is expected to serve over 107 connected devices/km2 by

		2030, powering the industrial internet-of-things era. Reconfigurable intelligent surfaces (RIS) are ideal low C-SWaP technology with supreme functional scope. RIS is essentially an array of 2D metallic scatters that can be reconfigured independently to control the local phase of the incident THz waves. At a far-field, the interference from all the scatters will effectively form the desired THz beam profile. However, practical demonstration of efficient THz RIS is still lacking. In this project, we will develop a MEMS-based programmable THz metasurface as an efficient RIS solution. The MEMS actuator integrated in the scatters will enable nW-level local phase control and the RIS with over 10,000 such elements will enable 3D beam steering in far-field. The THz RIS will be fabricated on 8-inch wafers using CMOS compatible foundry process. For addressing each of the 10,000 unit cells, ASIC will be developed and integrated with MEMS metasurface. This is essential to realize software programmable functionality of the RIS and provides a pathway for adopting AI-powered control of RIS.
Dr. Vishnu Paramasivam	RISC-V SoC with Energy Efficient CGRA Hardware Accelerator for Edge AI	The project goal is to design an innovative RISC-V CPU based parallel computing multi-core chip that achieves 50X improvement in energy-efficiency (performance per watt) in the edge devices. This aggressive goal is achieved by making a fundamental paradigm shift from the inherently sequential computing models to the naturally parallel dataflow model in advanced computing systems design. The multi-disciplinary research program is organized around five crosscutting thematic areas encompassing the computing stack: challenging applications, unconventional computing model, powerful compiler, innovative computer architecture, and advanced low-power circuits.

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