

## FACT SHEET

### **A\*STAR'S INSTITUTE OF MICROELECTRONICS TEAMS WITH MAJOR INDUSTRY PLAYERS IN HIGH DENSITY SYSTEM-IN-PACKAGE CONSORTIUM FOR HETEROGENEOUS CHIPLETS INTEGRATION**

**08 JULY 2021**

A\*STAR's Institute of Microelectronics (IME) announced a collaboration with four leading industry players to form a System-in-Package (SiP) consortium. IME will team with Asahi-Kasei, GLOBALFOUNDRIES® (GF®), Qorvo and Toray to develop high density SiP for heterogeneous chiplets integration that can meet the semiconductor industry's challenge in 5G applications. The newly formed consortium will leverage IME's expertise in FOWLP/2.5D/3D packaging.

Electronic system scaling is an industry trend driven by the need to pack increasing functionality and performance, at lower power consumption, into smaller form factors for a variety of consumer and enterprise applications such as 5G, artificial intelligence (AI) and high-performance computing (HPC) applications. To accelerate this trend, the consortium has embarked on a joint development programme to establish heterogeneous chiplet integration. The programme collectively addresses the companies' market requirements to integrate multiple system functions at the package level and achieve advanced SiP. Increasingly, the semiconductor industry is looking to SiP implementation to overcome the challenges of system integration posed by using traditional monolithic System-on-Chip (SoC) approaches or board-level integration techniques. Achieving this requires the industry to address design, processing, and materials challenges – with the collaboration members' aim to address in this consortium project.

#### **Leveraging 3D Integration Technologies for 5G Applications**

In 5G applications, multiple frequency band operation requires 5G devices to integrate numerous devices such as filters, Low Noise Amplifier (LNA)/ RF Switch, ASICs to support mobile communication and data-transmission over a range of frequency bands. This trend is expected to continue in the coming years, and results in increasing board-space consumed by Radio Frequency Front End (RFFE) modules used in 4G, 5G handsets. 3D Integration is an ideal way to integrate multiple devices/chiplets inside a small-form factor package. IME is teaming with consortium members to apply 3D integration technologies to miniaturise RFFE modules for 5G applications.

IME has invested in 3D integration technologies over the years, including Through-Si-Via (TSV). Over the past decade, IME has developed key process-modules, package-integration schemes, and design enablement to allow the industry ecosystem to harness the strengths of advanced packaging to achieve miniaturised systems. Key process modules that IME has developed include TSV, Through-Silicon-Interposer (TSI), fine-pitch multilayer Re-Distribution Layer (RDL), Micro-bumping, Wafer-to-Wafer (W2W), and Chip-to-Wafer (C2W) bonding, Wafer reconstruction, Thin-wafer handling, and more.

Package integration schemes supported by IME include 3D stacking using TSV first/middle/last followed by C2C, C2W and W2W; 2.5DIC using TSI; RDL-1st Fan-Out-

Wafer-Level Packaging (FOWLP); Chip-1st FOWLP; Antenna-in-Package for RF/mmWave; Ultra-thin Fan-Out Package-on-Package, and more.

To enable fabless companies to design Power-Performance-Area-Cost (PPAC) optimised packaging solutions, IME has developed the Package Process Design Kits (PDK) that support the above integration schemes. IME's PDK includes accurate package interconnect models for Signal/Power Integrity, and physical-verification enablement including Package DRC, LVS to facilitate package design signoff. In this consortium, IME will be applying these advanced packaging techniques to deliver package integration solutions for 5G applications.

“Together with our consortium members, we are committed to bringing advanced packaging solutions to the next level. IME's deep capabilities in 3D integration technologies will help accelerate the development of heterogeneous chiplets integration in high performance computing (HPC), 5G and AI applications, to advance the semiconductor industry,” said Prof Dim-Lee Kwong, Executive Director of IME.

“GLOBALFOUNDRIES is delighted to participate in this SiP Consortium for heterogeneous chiplets integration where chips fabricated using GLOBALFOUNDRIES advanced technologies will be integrated using new SiP technologies to miniaturize RFFE modules for 5G applications.” commented Dr. Siah Soh Yun, Vice President, TD, of GF.

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#### **About the Institute of Microelectronics (IME)**

The Institute of Microelectronics (IME) is a research institute of the Agency for Science, Technology and Research (A\*STAR). Positioned to bridge the R&D between academia and industry, IME's mission is to add value to Singapore's semiconductor industry by developing strategic competencies, innovative technologies and intellectual property; enabling enterprises to be technologically competitive; and cultivating a technology talent pool to inject new knowledge to the industry. Its key research areas are in Heterogeneous Integration, System-in-Package, Sensor, Actuators and Microsystems, RF & mmWave, SiC/GaN-on-SiC Power Electronics, and MedTech. For more information on IME, please visit [www.ime.a-star.edu.sg](http://www.ime.a-star.edu.sg).

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