JOINT RELEASE

SINGAPORE'S INSTITUTE OF MICROELECTRONICS AND CHARTERED DEVELOP ADVANCED FINE-PITCH PACKAGING SOLUTIONS AT 65NM

Singapore, 18 November 2008 – A*STAR's Institute of Microelectronics (IME), Singapore and Chartered Semiconductor Manufacturing (Nasdaq: CHRT and SGX-ST: Chartered), one of the world's top dedicated semiconductor foundries, have successfully optimized a range of fine-pitch packaging technologies for copper metallization and low-k dielectric silicon processes at 65 nanometer (nm) and below.

The Chartered-IME collaboration has led to a greater understanding of chip-package interaction of low-k devices through modeling, simulations and reliability verifications on silicon. When the collaboration began, there were no manufacturing-worthy fine-pitch packaging solutions available due to implementation challenges and the complex interaction between the silicon and packaging technology. The collaboration's results provide package designers with benefits from silicon-proven solutions and modeling tools to characterize the impact of fine-pitch package on silicon early in the design development cycle, which should improve manufacturability and back-end-of the-line yield performance.

"By leveraging IME's proven expertise in backend packaging know-how along with Chartered's success in advanced copper metallization and low-k dielectric process manufacturing, we have delivered a low-cost, high-performance solution that addresses key back-end integration challenges and provides a reliable path at 65nm from manufacturing to final chip packaging," said Dr. John H. Lau, Director of Microsystems, Modules & Components Laboratory of IME. "This research collaboration has brought much greater recognition to IME's packaging research works. Most notably, our research on the polymer encapsulated dicing lane technology (PEDL) provides better solutions for fine pitch copper low-k packaging."

"Chartered is committed to aggressively pursuing leading-edge research and development that can drive industry-leading technology and reliable solutions for our customers. By leveraging the joint silicon-proven, fine-pitch packaging solutions, our customers at 65nm and beyond could realize important volume ramp and time-to-market benefits from our collaboration with IME," said Sohn Dong Kyun, Senior Director, Integration Technology Division of Chartered.

The research, based on the 65nm processes developed by Chartered and its joint development partners, successfully developed a highly moisture-resistant surface mount plastic encapsulated Flip Chip Ball Grid Array (FCBGA) package for a 65nm copper low-k device. The research team achieved JEDEC Moisture Sensitivity Level 2 classification for a 13000+ I/O FCBGA at 40 x 40 mm^2 in package size. The team believes the achievement is the first-of-its-kind for the industry. The size of the 65nm copper low-k die is 21 x 21 mm^2 with a flip chip bump pitch of 150 microns (um). The package bill of materials are compatible for copper low-k die with Lead-Free and high lead bump assembly processing. One of the key advancements is that the package design exceeds JEDEC reliability requirements can be attributed to the established capability for mechanical dicing of 65nm copper low-k wafers. With Passivated Encapsulated Dicing Lane (PEDL) technology, the team believes that could offer more flexibility in narrower dicing lane and smaller crack stop design in future and more advanced CMOS technology node.

Chartered customers can learn more about accessing this technology through their turnkey representative.

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Notes to the Editor:

About Institute of Microelectronics (IME) www.ime.a-star.edu.sg

The Institute of Microelectronics (IME) is a research institute of A*STAR. Positioned to bridge the R&D between academia and industry, IME's mission is to add value to Singapore's semiconductor industry by developing strategic competencies, innovative technologies and intellectual property; enabling enterprises to be technologically competitive; and cultivating a technology talent pool to inject new knowledge to the industry. Its key research areas are in integrated circuits design, advanced packaging, bioelectronics, MEMS, nanoelectronics and photonics.

About Chartered

Chartered Semiconductor Manufacturing Ltd. (Nasdaq: CHRT, SGX-ST: CHARTERED), one of the world's top dedicated semiconductor foundries, offers leading-edge technologies down to 65 nanometer (nm), enabling today's system-on-chip designs. The company further serves its customers' needs through a collaborative, joint development approach on a technology roadmap that extends to 22nm. Chartered's strategy is based on open and comprehensive design enablement solutions, manufacturing enhancement strategies, and a commitment to flexible sourcing. In Singapore, the company operates a 300mm fabrication facility and five 200mm facilities. Information about Chartered can be found at www.charteredsemi.com.

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