Institute of Microelectronics
A*STAR

MEDIA RELEASE
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A*STAR'S IME LAUNCHES CHIP-ON-WAFER CONSORTIUM II AND COST-EFFECTIVE INTERPOSER CONSORTIUM TO ADVANCE CHIP PACKAGING SOLUTIONS FOR HIGH-VOLUME MANUFACTURING

Industry-focused consortia will address key challenges in wafer-level packaging to lower overall manufacturing costs and accelerate time-to-market of next-generation electronic devices

Singapore — A*STAR's Institute of Microelectronics (IME) has partnered leading semiconductor companies to develop cost-effective solutions in 2.5D and 3D wafer-level integrated circuit (IC) packaging. The newly formed Chip-on-Wafer Consortium II and the Cost-Effective Interposer Consortium will leverage IME's expertise in 3D and 2.5D IC integration; bonding technologies; as well as the design and packaging of semiconductor dies to develop advanced chip packaging solutions. All these capabilities will lead to cost savings and high-volume manufacturing.

In today's mobile and connected world, consumers demand next-generation devices that are multi-functional, more compact, offer better performance, and consume less power. As the industry moves towards more innovative technologies to keep pace with market trends, it must also keep manufacturing costs low to remain competitive.

The Chip-on-Wafer (CoW) Consortium II will build on the success of the first CoW consortium to further reduce production time and costs for 3D and 2.5D packaging. In the CoW Consortium I, IME and its partners successfully demonstrated Chip-on-Wafer bonding with Copper-Copper (Cu-Cu) diffusion bonding technology. The two-step process involves temporary flip-chip bonding and permanent gang bonding at a temperature of 200 degree celsius. This enables the scaling of the interconnect pitch of the integrated circuit from the average of 40 (micrometers) µm to 6µm.

The consortium achieved the highest throughput bonding – five times faster than the conventional solder-assisted thermo-compression bonding technique – making the flip-chip bonding of thin (20µm) through-silicon via (TSV) dies possible without damaging the chip.

These technological breakthroughs will allow device manufacturers to better integrate 3D chipsets such as complementary metal-oxide semiconductor (CMOS) image sensors, signal processors, logic and memory, and memory stacks. They will also increase the overall throughput by 400 to 500 per cent and lower the manufacturing cost by approximately 40 per cent.

The CoW Consortium II (please refer to **Annex A** for list of consortium members) will further develop the Cu-Cu diffusion bonding technology for energy-efficient and highly reliable devices. This technology will be applied in the development of 3D memory stack and 2.5D integration of a field-programmable gate array (FPGA) and memory on TSV-less interposer. It aims to achieve these by demonstrating a low-temperature Cu-Cu bonding with narrow-gap (3 to 5µm) flip-chip bonding, where the narrow gap is filled with optimised pre-applied under-fill.

Prior to the Cost-Effective Interposer Consortium, IME's 2.5D Through-Silicon Interposer (TSI) Consortium successfully demonstrated an end-to-end design-process-assembly-packaging flow for large area (39 mm by 27 mm) TSI with dense multi-level Cu interconnects. FPGA and Dynamic Random Access Memory (DRAM) ICs were integrated for high-performance and power-efficient systems. The consortium also developed a 2.5D TSI process design kit (PDK) and electronic design automation (EDA) flow for fabless companies to design TSI, and subsequently perform wafer fabrication, assembly and packaging at IME's 300mm wafer fabrication facility. These achievements afford companies across the value chain a lower cost of entry, and seamless design-to-manufacturing flow for 2.5D TSI technology. IME worked closely with Foundry, OSAT, Materials, Equipment, EDA, Fabless partners to capture their design and manufacturing requirements, and overcome challenges associated with the volume production of 2.5D TSI.

The Cost-Effective Interposer Consortium (please refer to **Annex B** for list of consortium members) will address the high manufacturing costs of interposers. It will address the capability limitations in silicon interposers for FPGA and graphic processing unit (GPU) IC designs for 2.5D and 3D IC packaging. IME and its partners will integrate value-added analog and power management unit (PMU) to the silicon interposer and develop an interposer which will not require TSV processing; hence reducing the cost of silicon interposers by up to 50 per cent.

Prof. Dim-Lee Kwong, Executive Director of IME said, "The outstanding results of phase 1 of our past consortia bring us to a new milestone in advanced chip packaging. They will play a foundational role in meeting challenging requirements for highly integrated mobile applications and connected devices. Moving forward,

I am confident that IME's close collaboration with our partners will continue to take our advanced packaging technologies and solutions to greater heights, and spur the mass adoption of cost-effective high performance systems."

Quotes from Industry Partners:

Lena Nicolaides, Vice President and General Manager of SWIFT Division, KLA-Tencor:
"Our strategic alliance with IME and industry partners has allowed us to tackle complicated process challenges in system design. This advances our yield management and process control strategies for production of devices with better functionality, lower cost and lower power consumption. We look forward to contributing our expertise in inspection and metrology in the Chip-on-Wafer Consortium II, and the Cost-Effective Interposer Consortium, as we further develop commercial solutions for the industry."

Tong Liang Cheam, Vice President of Advanced Packaging Business Line & Corporate Strategy, Kulicke & Soffa:
"We are pleased to be collaborating with IME on this Chip-on-Wafer Consortium II. K&S is confident that with the combined experience and knowledge, the consortium will extend the capabilities of Chip-on-Wafer (CoW) assembly and drive the solutions for yield improvements, cost reductions and ultimately broad market adoption."

Shim Il Kwon, Chief Technology Officer, STATS ChipPAC:
"Interposers provide a flexible, cost effective approach for the integration of heterogeneous dies from different technology nodes with advantages in miniaturisation, thermal performance and fine line width/spacing in a semiconductor package. We have found success in 2.5D integration using our fan-out wafer level technology and look forward to working with the Cost-Effective Interposer Consortium to drive a wider adoption and implementation of 2.5D solutions."

Rick Burns, Vice-President of Engineering, Semiconductor Test Division, Teradyne:
"Teradyne is pleased to join the Cost-Effective Interposer Consortium under the leadership of the IME. This is Teradyne's first opportunity to work with an IME consortium and we look forward to providing test design and test execution solutions to the consortium members. We expect to develop unique test techniques which will become standards for the industry as these new packaging solutions move from R&D and into production."

Yuichi Abe, Vice-President and General Manager, Tokyo Electron Ltd., ATSBU:
"Wafer level bonding is an emerging technology that has a huge potential to overcome various process limitations in semiconductor packaging. Our R&D collaboration with IME in wafer level bonding technology has proved to be rewarding with the successful demonstration of high throughput two-step chip-on-wafer bonding method. IME's expertise in the packaging technology and its state-of-the-art facilities will expedite the development and time-to-market of semiconductor equipment. We look forward to developing a wide range of bonding technologies which include high accuracy fusion bonding for 3D stacking and eutectic bonding for various MEMS applications."

S.R. Sheu, Vice-president and Co-chair of the Through-Silicon-Via (TSV) Committee, United Microelectronics Corporation (UMC):
"UMC is happy to contribute its extensive knowledge and experience in Through-Silicon Interposer to the Cost-Effective Interposer Consortium. By verifying IME's design concept on UMC's foundry manufacturing, we are building the foundation for a robust production source for this technology that will deliver performance, scaling and power saving advantages to chip designers using this TSI process. We look forward not only to bringing this effort to fruition, but also exploring further synergies between UMC and IME for additional opportunities."

Enclosed:

ANNEX A – Industry Members of the Chip-on-Wafer Consortium II
ANNEX B – Industry Members of the Cost-Effective Interposer Consortium

For media queries and clarifications, please contact:

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About the A*STAR Institute of Microelectronics (IME)

The Institute of Microelectronics (IME) is a research institute of the Science and Engineering Research Council of the Agency for Science, Technology and Research (A*STAR). Positioned to bridge the R&D between academia and industry, A*STAR IME's mission is to add value to Singapore's semiconductor industry by developing strategic competencies, innovative technologies and intellectual property; enabling enterprises to be technologically competitive; and

cultivating a technology talent pool to inject new knowledge to the industry. Its key research areas are in integrated circuits design, advanced packaging, bioelectronics and medical devices, MEMS, nanoelectronics, and photonics.

For more information on IME, please visit www.ime.a-star.edu.sg.

About the Agency for Science, Technology and Research (A*STAR)

The Agency for Science, Technology and Research (A*STAR) is Singapore's lead public sector agency that spearheads economic oriented research to advance scientific discovery and develop innovative technology. Through open innovation, we collaborate with our partners in both the public and private sectors to benefit society.

As a Science and Technology Organisation, A*STAR bridges the gap between academia and industry. Our research creates economic growth and jobs for Singapore, and enhances lives by contributing to societal benefits such as improving outcomes in healthcare, urban living, and sustainability.

We play a key role in nurturing and developing a diversity of talent and leaders in our Agency and Research Institutes, the wider research community and industry. A*STAR oversees 18 biomedical sciences and physical sciences and engineering research entities primarily located in Biopolis and Fusionopolis.

For more information on A*STAR, please visit www.a-star.edu.sg.

ANNEX A

INDUSTRY MEMBERS OF THE CHIP-ON-WAFER CONSORTIUM II:

- Altera Corporation
- KLA-Tencor *
- Kulicke & Soffa
- Panasonic Corporation, Automotive & Industrial Systems Company, Electronic Materials Business Division
- Panasonic Factory Solutions, Asia Pacific*
- SanDisk
- Sony Semiconductor Solutions
- Tokyo Electron Ltd.*
- Toray Industries, Inc.

* Companies which have participated in the Chip-on-Wafer Consortium I

ANNEX B

INDUSTRY MEMBERS OF THE COST-EFFECTIVE INTERPOSER CONSORTIUM:

- Altera Corporation**
- Inotera Memories, Inc.
- KLA-Tencor
- Picosun
- STATS ChipPAC Limited
- Teradyne Corporation
- Tessolve Semiconductor Pvt. Limited
- Tokyo Electron Ltd
- United Microelectronics Corporation (UMC)**
- Veeco Instruments, Inc.

** Companies which have participated in the 2.5D Through-Silicon Interposer (TSI) Consortium