Institute of Microelectronics
A*STAR

MEDIA RELEASE
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A*STAR'S IME KICKS OFF CONSORTIA TO DEVELOP ADVANCED PACKAGING SOLUTIONS FOR NEXT-GENERATION INTERNET OF THINGS APPLICATIONS AND HIGH-PERFORMANCE WIRELESS DATA TRANSFER TECHNOLOGIES

Innovative capabilities developed will lead to higher power efficiency and lower costs for MEMS and silicon photonics devices

Singapore — A*STAR's Institute of Microelectronics (IME) has launched two consortia on advanced packaging, the Silicon Photonics Packaging consortium (Phase II) and the MEMS Wafer Level Chip Scale Packaging (WLCSP) consortium. They will develop novel solutions in the heterogeneous integration of micro-electromechanical systems (MEMS) and silicon photonics devices, which will boost overall performance and drive down production costs. The new consortia will leverage on IME's expertise in MEMS design, fabrication, wafer level packaging process, as well as silicon photonics packaging modules and processes.

The proliferation of the Internet of Things (IoT) is driving the rapid growth of diversified technologies which are key enablers in major application domains such as smart phones, tablets, wearable technology; and network infrastructures that support wireless communications.

However, this trend requires the complex integration of non-digital functions of 'More-than-Moore' technologies such as MEMS with digital components into compact systems that have a smaller form factor, higher power efficiency and cost less. The onset of big data, cloud computing and high speed broadband wireless communications also calls for novel use of silicon photonics. Silicon photonics are a critical enabler of high density interconnects and high bandwidth, to meet high optical network requirements cost-effectively.

In the previous Silicon Photonics Packaging Consortium (Phase I), IME and its industry partners developed new capabilities in necessary device library and associated tool boxes to enable the integration of low profile lateral fibre

assembly, laser diode and photonics devices. By employing a laser welding technique, the consortium demonstrated a fiber-chip-fiber loss of less than 8 decibel (dB) with less than 1.5dB excess packaging loss. These capabilities enabled integrated silicon photonic circuits to provide higher data rates at lower cost and power consumption. For details, please refer to **Annex A.**

Building on these achievements, the Silicon Photonics Packaging Consortium (Phase II) will develop a broad spectrum of silicon photonics packaging methodology. The consortium will further develop low loss silicon coupling modules, and provide a series of packaging solutions for laser diode integration. It will also focus on developing accurate thermal models, as well as improve overall module thermal management, reliability and radio-frequency (RF) performance to meet very high data bandwidth demand. All these new developments will lead to a more integrated packaging solution which promises better assembly margins and lower module costs.

IME's MEMS WLCSP Consortium has also been established to develop a cost-effective integration packaging platform for capped MEMS and complementary metal-oxide semiconductor (CMOS) devices. This platform could be used for any MEMS devices with cavity-capping such as timing devices, inertial sensors, and RF MEMS packaging.

Conventional chip stacking that relies on a through-silicon via (TSV) and wire bonding on substrate method will usually result in high costs and large form factor. The consortium aims to lower production costs and achieve smaller footprint by developing a TSV-free over-mold wafer level packaging solution for MEMS-capped wafer using a novel metal deposited silicon pillar and wire bonding as a through mold interconnects.

The consortium aims to reduce form factor of integrated MEMS and CMOS devices by approximately 20 per cent, and lower manufacturing costs by approximately 15 per cent. These cost-effective packaging solutions are also expected to produce better electrical and reliability performance.

"These consortia partnerships play a critical role in developing innovative solutions to meet emerging market demands. Through these collaborations, we will elevate our capabilities from developing MEMS and silicon photonics devices to developing advanced solutions in heterogeneous integration. The capabilities developed will enable our industry partners to capture new growth opportunities in the IoT space and accelerate market adoption of cost-effective technologies," said Prof. Dim-Lee Kwong, Executive Director of IME.

"Silicon photonics packaging is a crucial technology for the commercialisation of silicon photonic devices. The partnership generated remarkable results in the Silicon Photonics Packaging Consortium Phase I, and we are pleased to continue with the second phase, which will expand the application of silicon

photonics with innovative approaches in terms of LD integration and RF performance. Through this consortium, Fujikura will accelerate the development of compact and cost-effective optical communications for diverse markets," said Mr. Kenji Nishide, Executive Officer, General Manager, Advanced Technology Laboratory, Fujikura Ltd.

"Currently, it is anticipated that the demand for sensors will grow from billions to trillions by 2050. This demand is being driven by the emergence of sensor based smart systems fusing computing, connectivity and sensing in the context of the Internet of Things. IME's packaging consortia partnership will allow us to identify and develop MEMS packaging innovative solutions in order to scale up for the Internet of Things," said Mr. Mo Maghsoudnia, Vice President of Technology and Worldwide Manufacturing of InvenSense.

Mr. Shim Il Kwon, Chief Technology Officer, STATS ChipPAC said, "As the number of MEMS devices in emerging IoT applications continues to grow, semiconductor packaging will have a significant impact on the performance, size and cost targets that can be achieved. By collaborating with our partners in the consortia, we will be able to help drive the cost effective integration of MEMS and ASICs in high performance, high yield WLCSP solutions for IoT products."

For information on the industry members of these consortia, please refer to **Annexes B and C** respectively.

Enclosed:

ANNEX A – Silicon Photonics Consortium (Phase I) Achievements

ANNEX B – Industry Members of the Silicon Photonics Packaging Consortium (Phase II)

ANNEX C – Industry Members of the MEMS WLCSP Consortium

For media queries and clarifications, please contact:

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About the A*STAR Institute of Microelectronics (IME)

The Institute of Microelectronics (IME) is a research institute of the Science and Engineering Research Council of the Agency for Science, Technology and Research (A*STAR). Positioned to bridge the R&D between academia and industry, A*STAR IME's mission is to add value to Singapore's semiconductor industry by developing strategic competencies, innovative technologies and intellectual property; enabling enterprises to be technologically competitive; and cultivating a technology talent pool to inject new knowledge to the industry. Its key research areas are in integrated circuits design, advanced packaging, bioelectronics and medical devices, MEMS, nanoelectronics, and photonics.

For more information on IME, please visit www.ime.a-star.edu.sg.

About the Agency for Science, Technology and Research (A*STAR)

The Agency for Science, Technology and Research (A*STAR) is Singapore's lead public sector agency that spearheads economic oriented research to advance scientific discovery and develop innovative technology. Through open innovation, we collaborate with our partners in both the public and private sectors to benefit society.

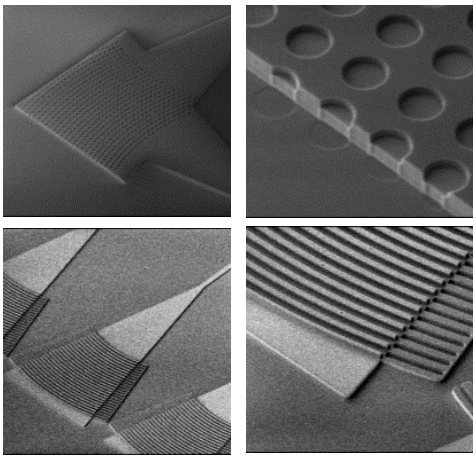
As a Science and Technology Organisation, A*STAR bridges the gap between academia and industry. Our research creates economic growth and jobs for Singapore, and enhances lives by contributing to societal benefits such as improving outcomes in healthcare, urban living, and sustainability.

We play a key role in nurturing and developing a diversity of talent and leaders in our Agency and Research Institutes, the wider research community and industry. A*STAR oversees 18 biomedical sciences and physical sciences and engineering research entities primarily located in Biopolis and Fusionopolis.

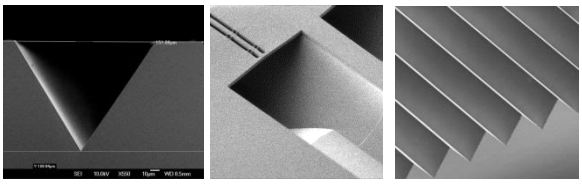
For more information on A*STAR, please visit www.a-star.edu.sg.

ANNEX A

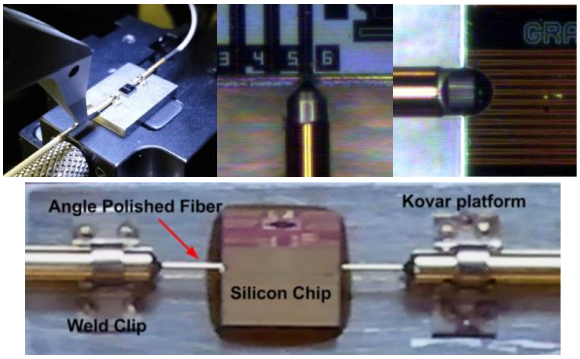
SILICON PHOTONICS CONSORTIUM (PHASE I) ACHIEVEMENTS



Silicon grating coupler: 2D grating to achieve polarisation diversity performance; Grating coupler with silicon overlay to reduce the coupling loss (<2.6 dB) on 220-nanometer (nm)-thick Silicon on Insulator (SOI)



Precision fiber groove formation



Lateral fiber assembly using laser welding technique: Fiber-to-fiber loss <8 dB, Excess loss <1.5 dB

ANNEX B

INDUSTRY MEMBERS OF THE SILICON PHOTONICS PACKAGING CONSORTIUM (PHASE II):

- Accelink Technologies Co. , Ltd.
- Corning Incorporated
- Fujikura Ltd.
- Fraunhofer Heinrich Hertz Institute
- NTT
- A High Speed Electronics Provider

ANNEX C

INDUSTRY MEMBERS OF THE MEMS WLCSP CONSORTIUM:

- Delta Electronics, Inc.
- InvenSense Inc.
- Standing Egg Inc.
- STATS ChipPAC Limited
- ULVAC, Inc.